NOVEMBER 1989

# COMPUTER

## SIMPLIFYING COMPLEXITY

### A Structured Approach for VLSI Circuit Design

Also in this issue

- Broadband ISDN
- Deadlock Detection
- Taulbee Survey
- Supercomputer Reports

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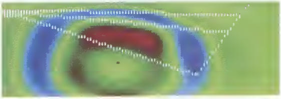

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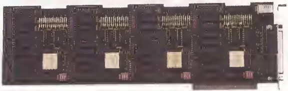

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Two reports from the IEEE Scientific Supercomputer Subcommittee: The first report traces and analyzes the evolution of computer classes and offers near-term projections; the second updates a 1983 report on supercomputer hardware.

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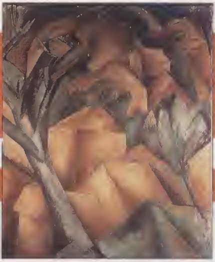

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Cover image: *Houses at L'Estaque*, a 1908 oil on canvas by Georges Braque, is on display at the Museum of Modern Art, New York. The exhibition, "Picasso and Braque: Pioneering Cubism," opened September 24, 1989, and runs through January 16, 1990. It brings together, for the first time, experiments in Cubism produced by the two artists in dialogue with each other. Their extraordinary collaboration created a revolution so sweeping that today, over 75 years later, its influences are still felt, not only in art but also in architecture, music, and literature.
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Cover design: Jay Simpson, Design & Direction

*IEEE Computing Futures*, 86-page supplement for students in Central and Northern California and libraries

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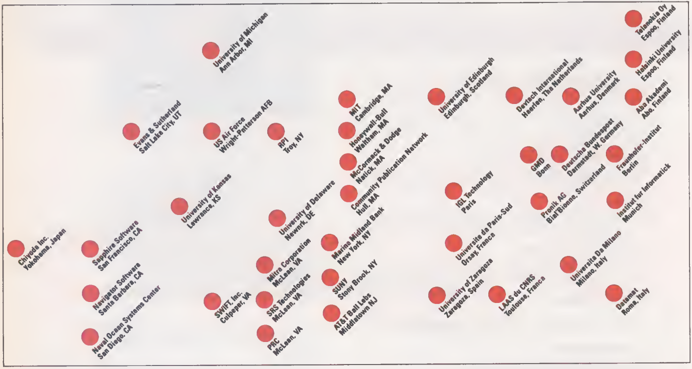

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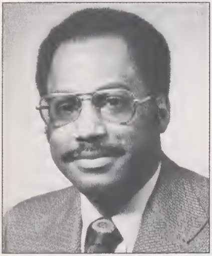

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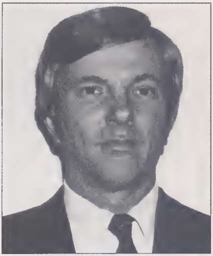

**Edward A. Parrish, Jr.**

# National High-Performance Computer Act deserves support

Affordable, universally available networking is a high priority for our profession. For this month's column, I've asked Past President Ed Parrish to tell you about legislation, currently under consideration by Congress, that could do much toward furthering this and other important goals of the computing and communications communities.

Kenneth R. Anderson
President

As some of you may be aware, a bill now under consideration in Washington could have tremendous impact on computer professionals as well as the general public. Known as the National High-Performance Computer Act, S. 1067, it was introduced earlier this year by Senator Albert Gore, Jr. (D-Tenn.), with identical legislation introduced in the House (HR 3131) by Representative Doug Walgren (D-Pa.). The bill consists of several sections addressing general issues associated with making supercomputers widely accessible to researchers, small and large businesses, manufacturers, and the educational establishment. It would authorize $1.75 billion over five years and could dramatically affect this nation's position as an international leader in developing and using high-speed computer technology. (For details, see "Update", p. 75).

Of particular interest to members of the Computer Society are Title II—National Research and Education Network (NREN) and Title VI—Basic Research and Education. Title II would direct the National Science Foundation to establish, with other federal agencies, a three-gigabit-per-second national network by 1996 with $400 million of funding through fiscal year 1994, commencing with $50 million in 1990. Title VI would authorize an additional $10 million in fiscal year 1990, growing to $50 million in 1994, to support attendant basic research in computer technology, computer science, electrical engineering, and materials science, and to educate researchers. Clearly, this bill should receive the support of the computer science and engineering community.

Senator Gore has likened the NREN to the interstate highway system, calling it an "interstate network of information superhighways." This new system would provide a high-capacity link between supercomputer centers and other facilities, with "interchanges" whereby users could gain access from other networks. This analogy is useful for explaining the NREN to lay people, but it also allows extrapolations concerning the likely benefits associated with the network. One reasonable view of the NREN is as an enabling technology that eventually

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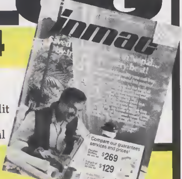

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To date, this country has some 60,000 miles of fiber optic cable operating at speeds from 405 megabits per second to 1.7 gigabits per second. By using wave division multiplexing, it is estimated that these rates could be quickly doubled. Recent improvements in optoelectronic devices are expected to allow driving such cable at 2.4 gigabits per second. By using multiplexing with these drivers, speeds approaching 4.86 gigabits per second should be attainable. These speeds have already been reached under laboratory conditions. Consequently, considerable groundwork for the NREN already exists, so the risk of failure, given sufficient resources, appears remote. Should the country fail to move expeditiously to implement the NREN, the risks are great and generally apparent.

One risk that computer professionals might be unaware of involves our ability to design and produce optoelectronic equipment. At present, foreign companies dominate the manufacturing of optoelectronic equipment. They are apt to be less than enthusiatic about our needs for specialized devices to help assure US leadership in the information age. Thus, it is crucial that we enhance our own capabilities on this and other technological fronts.

This past June, Senator Gore invited my participation in a working session following a hearing on "Supercomputing and Information Superhighways" before the Science, Technology, and Space Subcommittee. There were about two dozen invitees drawn primarily from the computer and telecommunication industries. At both the hearing and the subsequent meeting, there was widespread support for this bill and a sense of urgency over the need to convince legislators and the public of the necessity for the recommended actions.

This is where you come in. There is no stronger lobbying effort than letters written by constituents to their elected officials in Washington. I urge you to find out more about this bill and form your own opinion. I hope you will join with me and many others in our profession in lending your much-needed support. Mail to your senator or representative can be addressed to Senate, Washington, DC 20510 or to House, Washington, DC 20515.

Edward A. Parrish, Jr.
Past president

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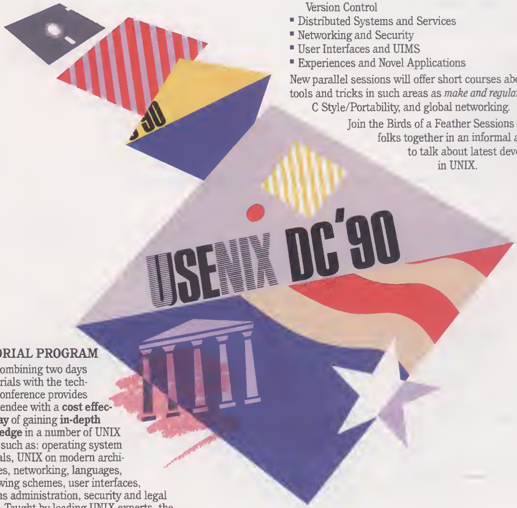

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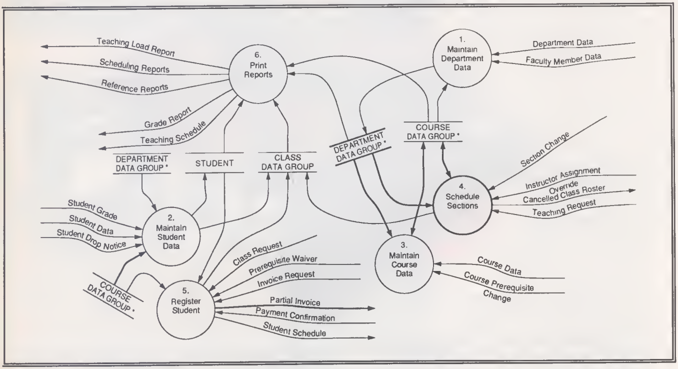

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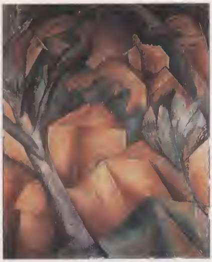

# A Structured Approach for VLSI Circuit Design

**Jun Gu and Kent F. Smith**
**University of Utah**

Designing large, complex integrated circuits with millions of transistors requires the extensive use of computer aids. A structured design method is of major importance for managing the complexity of very large scale integration issues and automating the computer-aided IC design process.[1,2]

Performance, cost, features, and time to market are the critical factors that separate winners from losers in the IC market. Not coincidentally, these same pressures also affect vendors of integrated circuit CAD systems. Structured design techniques offer a quick, cost-effective, and user-friendly way to deliver a circuit from its logic design to real fabrication.

The following facts — obtained by private communication with Paul Losleben in April 1988 at the Center for Integrated Systems at Stanford University — demonstrate the viability of structured design techniques:

(1) Of an estimated 500,000 electronic designs performed in the US during 1987, about 18,000 of them were custom or semicustom ICs. Of those, 70 percent (47 percent gate arrays and 23 percent standard cells) were designed using structured, semicustom design techniques.

(2) The growth rates for gate-array design, standard-cell design, and full-custom design were plus 33 percent, plus 70 percent, and minus 9 percent, respectively.

**The growing functional complexity of VLSI circuit design demands a simple, structured design method. Students using PPL can implement MOS or GaAs VLSI circuits with 100,000 transistors in a few weeks.**

First we will review the research done on a structured, symbol-based IC design method called Path Programmable Logic. Then we will explain the justification behind the basis for the PPL method. The design methodology reported here primarily results from a long-term research effort over the past 10 years on the part of students and faculty in the VLSI Group at the University of Utah.

Compared to full-custom design methods, the PPL method permits an order of magnitude reduction in design time. In most cases, the density of the circuits designed using the PPL method approaches or surpasses that of the practical full-custom designs. Compared to semicustom design techniques such as standard cells and gate arrays, PPL reduces the design time by a factor of three while improving the densities by a factor of two to three.

## Conventional versus PPL IC design

In general, the design of a conventional integrated circuit includes five phases:

(1) specification,
(2) functional design,
(3) logic design,
(4) circuit design, and
(5) physical design.

Each design phase is characterized by synthesis, analysis, and verification. During the design process, three different representations are commonly used to show different aspects of the system under design.[1,3] *Behavioral representations* describe a circuit's function. *Structural representations* describe the composition of the circuit in terms of cells, components, and interconnections among the components. *Physical representations* are characterized by information used in the manufacture or fabrication of physical systems.

Designers have long realized that, to facilitate IC design, they need a computer-aided design tool that encapsulates different levels of the design phases, ranging

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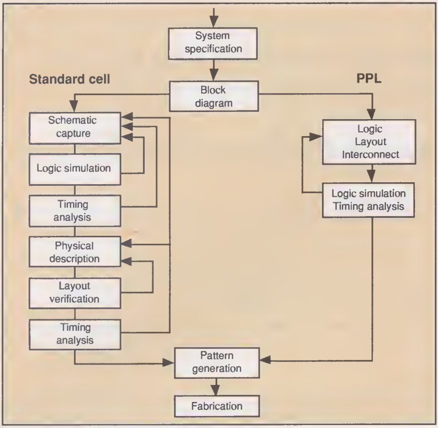

**Figure 1. Standard-cell design method versus the PPL design method.**

from low-level composite layout through middle-level schematic and logic design to high-level symbolic manipulation. For rapid VLSI design, we need a tool that operates completely on a symbolic layout level and avoids the lower level details. The structured design method described below can provide consistent descriptions in the three design representations (behavioral, structural, and physical) at all relevant levels of abstraction.

**Path Programmable Logic.** Research by the VLSI Group at the University of Utah during the past several years has resulted in a symbolic, structured, and technology-independent IC design method known as PPL.[4,5] We developed this method in response to the need for an IC design method that takes less time than full-custom design techniques while maintaining a high transistor density. PPL fulfills both of these requirements and has other significant advantages as well.

PPL uses a cell matrix method that places cells at arbitrary locations. Interconnection is accomplished by placing cells next to each other; connections are made across all four sides of the cells. Elementary cells perform AND and OR operations for a programmable logic array. The AND conditions of the input signals form on the rows of the PPL circuit and the OR conditions form on the columns.

Cells in addition to those needed to perform the sum-of-products realization of a function are also provided. These include flip-flops, inverters, loads, row and column connections, and pass transistors. Consequently, you can easily design both combinational and sequential circuits (see "Introduction to the PPL design method" below). You can custom design the PPL circuits to optimize performance and size for the chosen IC process.

Using the PPL method, you would design a circuit by placing symbols representing cells on a grid representing the integrated circuit. A completed grid corresponds to the logical representation, the structural representation, and the physical representation of the circuit.

The PPL method of representing the circuit saves many steps in the design process. Figure 1 illustrates the design of a circuit using standard cells versus the design using the PPL method. The design of a circuit using standard cells has a distinct separation between the logical design and the physical design. In the standard cell design, the steps of schematic capture, logic simulation, and approximate timing analysis are completely independent of the physical steps, which include physical design, layout verification, and exact timing analysis.

Typically, you would iterate your design at the logical level until you meet the requirements, then move to the physical design. If the physical design does not meet the required specifications, you would reiterate the design. It might be, for example, that the wiring capacitance resulting from the automatic placement of the standard cells is too large and yields unacceptable performance, or perhaps the resulting wire length causes unacceptable distortion of the signals. These conditions might require new iterations of the logical design.

This standard cell design style results in a large number of steps in the design process, with many of the design steps essentially unrelated. In the PPL design method, functional design, logic design, circuit design, and physical design have been combined into one step, thereby reducing the number of design steps and increasing design productivity. For example, in PPL the designer controls layout topology at the time of logic design, thus allowing the logic designer, not an automatic placement program, to control the circuit delays directly.

## Introduction to the PPL design method

PPL circuits are built on a "sea-of-wires," as shown in Figure 2. Instead of thinking of an IC as initially covered with a sea of transistors or gates that can be interconnected with wires, the PPL method views the IC as a set of horizontal and vertical wires into which you can place transistors or gates. You can manually or automatically connect wires at any cross point or break a wire.

To lay out a PPL cell, as illustrated in Figure 3, you simply remove the existing wires and replace them with a predefined circuit. You can leave the interconnecting wires on all four sides intact or remove them to form interconnections to other cells. Power and ground supply wires run on the bottom level of interconnect to all grid locations, but their presence is invisible to the user.

The smallest cells cover exactly one unit cell area and are called *unit cells*. The cells that take more than one unit area are called

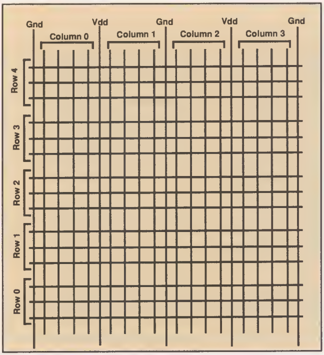

Figure 2. Blank PPL layout plane.

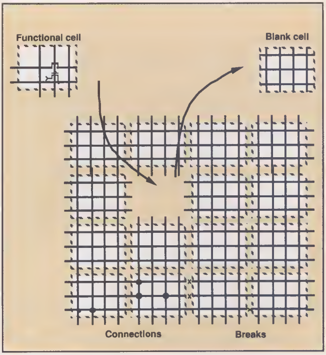

Figure 3. Placement of a cell onto the PPL layout plane (CMOS).

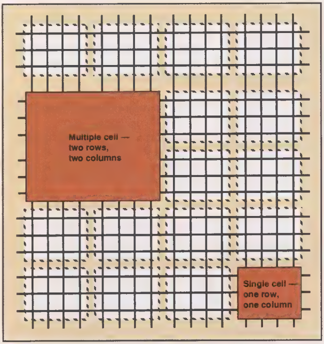
Multiple cell — two rows, two columns
Single cell — one row, one column

Figure 4. PPL unit cell and complex cell.

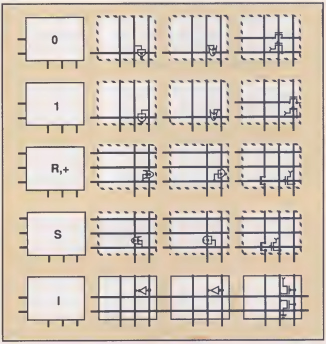

Figure 5. Symbolic and schematic representations of several basic PPL cells.

*multiple cells*, as shown in Figure 4. Multiple PPL cells may include circuits as simple as a flip-flop or as complicated as a reduced instruction set computer module.

PPL cells are the key to the performance of VLSI circuits and systems designed using the PPL method. At the lowest composite layout level, they must meet circuit logic schematic and electrical specifications as well as multiple topological connections. At the higher symbolic logic design level, their symbolic representation must support a general, rule-based, hierarchical, and technology-independent IC design method.

Currently, two N-channel metal-oxide semiconductor technologies, four complementary MOS technologies, and two gallium arsenide technologies have been developed for the PPL cell sets. (For details of NMOS, CMOS, and GaAs PPL cell implementations, see our technical reports.[6,7]) The basic PPL cells — 1, 0, S (set), R (reset) — appear in Figure 5. They

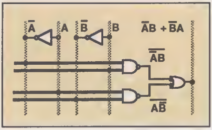

**Figure 6. Conventional schematic of EXOR gate.**

are all unit cells, the building blocks from which we can make almost any circuit.

You can best understand the design of PPL circuits by examining some simple PPL circuit designs. Two examples follow, an EXOR (combinational) circuit and a binary counter (sequential) circuit.

**An EXOR circuit design using PPL.** Figure 6 shows the schematic of a conventional EXOR gate. Using the 0 and 1 PPL cells, Figure 7 shows a PPL logical representation of the NAND gate used in the construction of the PPL EXOR gate. One can see from Figure 7b that the conventional NAND gate in Figure 7a is "split" into two parts and represented as distributed logic. This "splitting" allows a simple PPL cell to replace the PPL distributed logical component. Figure 7c shows the symbolic PPL cells for the NAND gate, while Figure 7d shows the predefined schematic.

The PPL tools automatically route the NAND gate (including "short" connections, ground connections, and routing between PPL cells). The process is transparent to the designer. You can isolate the complete NAND circuit as a module by breaking the wires around the edges of the circuit.

Figure 8 shows how you can construct the complete EXOR circuit using four different PPL cells. The corresponding PPL distributed logical representation and PPL circuit schematic appear in Figures 9 and 10. As a practical matter, the PPL library of cells includes an EXOR cell that performs the EXOR function, so we use this example for illustration only.

**A binary counter design using PPL.** The sequential circuit design example is a binary counter. Figure 11 gives the counter's state transitions. To better understand the counter circuit design, we will first examine a programmable logic array implementation of the circuit. This PLA design appears in Figure 12. The circuit consists of three structures: the AND plane, the OR plane, and the state variable memory, the Memory plane. The inputs to the AND plane enter on column wires, and the outputs exit on row wires. The inputs to the OR plane enter on row wires, and the outputs exit on column wires. We assume that the column signals will be true when high; that is, 1 = high. Each of these three parts is compact in itself, but we cannot merge them into a single, coherent structure.

The conventional PLA method has the distinct disadvantage, therefore, of having three independent physical planes that are difficult to integrate together. If we fold the AND and OR planes onto one plane, we obtain the structure illustrated in Figure 13. The output columns have been interspersed with the input columns. We can now view the folded planes as a single grid, with each location containing either AND elements, OR elements, or memory elements as shown by the boxes.

Notice that none of the O's or X's fall on top of each other. If they did, for example, you would detect that the state of a flip-flop was a 1 and then act to set it. Conversely, you would not want to detect that the state of the flip-flop was a 0 and reset it.

Compared to a PLA design technique, this folded design shows a more flexible and coherent layout structure. It has the advantage of having all three planes (AND, OR, and Memory) occupying separate grid locations in which any logic element of any of the three planes can be placed at an arbitrary location.

If we now assign symbolic meanings to the O's and X's as shown in Figure 13, the counter design can be described in terms of simple rules. From the counter state transition sequence in Figure 11, we can derive three PPL design rules:

(1) If the state changes from 0 to 1, then do an S (set) operation.

(2) If the state changes from 1 to 0, then do an R (reset) operation.

(3) If the state does not change, then do nothing.

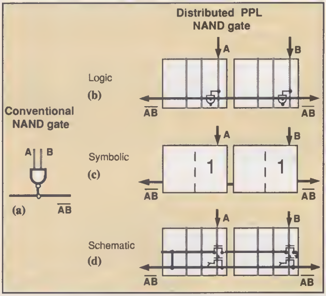

**Figure 7. Constructing a NAND gate using simple PPL cells.**

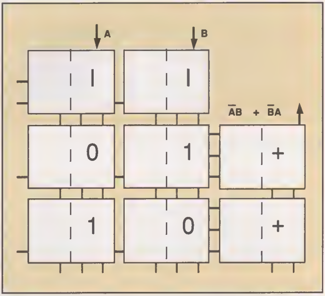

**Figure 8. PPL symbolic representation of EXOR gate.**

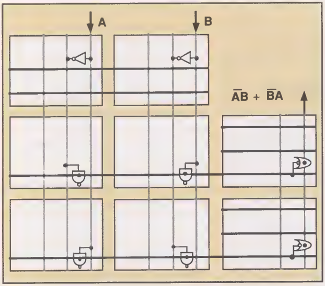

**Figure 9. PPL distributed logical representation of EXOR gate.**

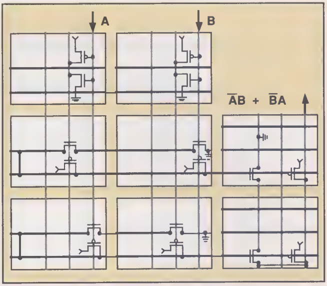

**Figure 10. PPL schematic representation of EXOR gate.**

For example, according to these rules, to perform state transition 2 (i.e., $Q_1Q_2$ from 01 to 10), the required high-level PPL symbolic representations are

(1) $Q_1$ from 0 to 1 implies a PPL layout of 0 S.

(2) $Q_2$ from 1 to 0 implies a PPL layout R 1.

Note that the S (set) operation is left-active (that is, S sets 0 to 1) and the R (reset) operation is right-active (that is, R resets 1 to 0) because of the physical layout of the flip-flop. In the PPL design method, any sequential circuit, such as the entire counter sequence in Figure 11, can be directly mapped into the PPL symbolic layout (see Figure 14) without tracing conventional state transition equations. Note that we have combined rows $R2$ and $R4$ into a single row, because $F2$ is always set whenever $F2$ and Enable are both 1; that is, $F2$ toggles regardless of the state of $F1$.

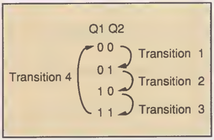

**Figure 11. Binary counter sequence.**

This CMOS binary counter example uses five CMOS PPL cells: 1, 0, S (set), R (reset), and F (flip-flop). In this case, the 1,

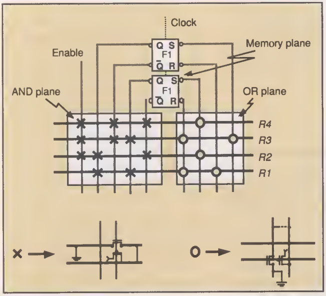

**Figure 12. PLA implementation of a binary counter.**

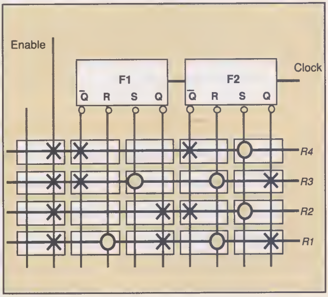

**Figure 13. PPL design of a binary counter.**

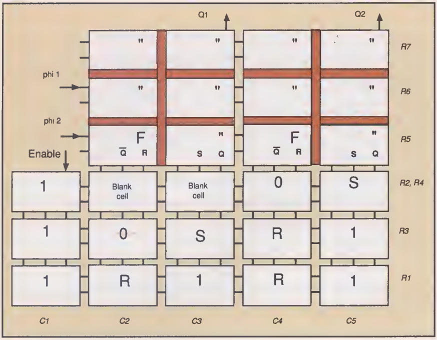

Figure 14. PPL symbolic layout for a binary counter.

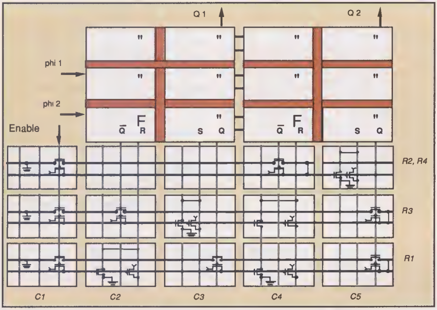

Figure 15. CMOS schematic of PPL binary counter circuit.

0, R, and S cells are unit cells. Figure 5 gives their schematics. The flip-flop cell F, a multiple cell, is composed of 2 × 4 or 8 total unit cells. Figure 15 illustrates the circuit schematic of the binary counter. (The extra interconnections for short-circuit and power and ground supply are automatically added by the PPL tools described below.) The CMOS logic schematic of the PPL cells also appears in Figure 15.

An automated CAD tool to generate PPL sequential circuits is available[8]; we give this example for illustration purposes only.

**Basic features of PPL design.** Among the many unique features of the PPL design method, the following aspects are significant:

(1) *Logic design by functionally conceptualized mapping.* Note that circuit logic design using PPL is a functionally conceptualized mapping rather than a schematically conceptualized design. For example, cell 0, or cell 1, senses column logic states and invokes a new row logic state. This forms an AND term in the PPL circuit and presents a rule in an If statement (like a noun, which represents an object in a rule statement). Similarly, cell S (set), or cell R (reset), sets a column logic state according to the current row logic state, which produces an OR term in a PPL circuit and generates a rule in a Then statement (like a verb, which represents an action in a rule statement).

As shown in the example of a binary counter given above, in most cases circuit synthesis using PPL can be done based on a straightforward and common understanding of the given circuit's functional specifications (e.g., the three rules above). The PPL symbols for the counter can be directly mapped onto the PPL grid.

(2) *Universal and flexible IC building blocks.* The details of the PPL logic partitioning scheme are described in the section "Partitioning for structured VLSI design" below. This logic partitioning scheme possesses a high degree of functional completeness and offers great structural regularity and design composability for general and less-redundant circuit design.

(3) *Hierarchical symbolic conceptual abstraction.* PPL has the unique advantage of giving a simultaneous high-level view of the symbolic representation, the logic, the schematic, the composite layout, and the interconnect of a VLSI circuit in a single step. This frees a designer from many labor-intensive and time-consuming low-level details (such as composite layout, the extraction of circuit schematics, design rule checks, etc.) during IC design.

(4) *Technology independence.* PPL design is technology independent. For example, by symbolically replacing the PPL cells in the technology database, you can easily transfer a PPL chip designed using NMOS technology into chips that will be fabricated using CMOS or GaAs technologies, or vice versa. The higher level PPL symbolic representation for NMOS, CMOS, and GaAs technologies remains almost the same.[9]

(5) *User-friendly interaction.* User-friendly interaction with the PPL system is a direct consequence of the above features. As we will discuss in the section "Practical assessment of the PPL design method," IC designers using the PPL design method can achieve an order of magnitude reduction or more in design time (as compared to other semicustom IC design techniques).

**PPL compared to other cell-based,**

**structured design methods.** Compared to PLA design techniques, the PPL method produces a more flexible and coherent layout structure. The PPL design method also differs in many ways from other structured, cell-based design methods.

Standard-cell and gate-array layout systems, for example, arrange the components in rows (columns can be transformed to rows by rotation). This is essentially a one-dimensional layout structure. The cells are designed to have a uniform height, and the width varies with the complexity of the cell. In these cases, the layout has rows of cells with spaces between the rows for interconnection. The structure of the PPL design, having interconnection on all four sides of each cell, provides the designer with a two-dimensional layout that offers flexible circuit composability.

General cell layout systems model the components in two dimensions, since both their height and width can affect the layout. However, general cell layouts are not restricted to having similar shapes and sizes, which adds considerable complexity. In PPL design, grid locations for cell placement are uniformly spaced. Each PPL cell is carefully partitioned and implemented with optimal regularity and consistency in the sense that a cell can be inserted onto any location on the layout plane without violating any local or global electrical and/or topological constraints.

The logic functions in the PPL layout are determined by the cells' relative placement. Thus, the PPL layout has the feature of flexibility instead of rigidity, as in other methods.

## Principles of the PPL design method

Logic partitioning and interconnection strategies are functions within structured, cell-based design methods. Logic partitioning determines the structure of the partitioned logic components. Interconnection strategy determines the compatibility and connectivity of the partitioned logic components.

Among many structured, array-based design methodologies such as ROMs, PLAs, gate arrays, standard cells, and general cell design, PPL distinguishes itself by its unique partitioning scheme and interconnection strategy.

**Partitioning for structured VLSI design.** A structure helps us effectively use both computer and human capabilities. The success of a structured IC design method depends on its logic partitioning scheme. A *logic partitioning scheme* divides a large logic circuit into a collection of smaller modules (or subcircuits) according to some criteria. It basically consists of two key components:

- Granularity — the minimum logic function performed by the smallest partitioned logic component. The granularity of a partitioned logic component could be coarse, large, small, or fine.
- Orthogonality — the functional independence among the smallest partitioned logic components. The ideal functional orthogonality enforces maximum functional independence among the set of smallest partitioned logic components. No component contains the others nor can it be replaced by the others. This feature avoids duplicated work in building IC circuit cells.

The logic partitioning scheme of a structured IC design method is one of the key factors that contributes to the technical merits of the design method. The following four aspects characterize the logic partitioning scheme:

(1) *Conceptual abstraction.* Conceptual abstraction replaces a partitioned logic component with a simplified model that defines the interaction of the partitioned component with its environment. Abstraction reduces the amount of data needed to describe a partitioned logic component and supports hierarchical decomposition and abstraction as well. Modularity (a well-defined, unambiguous functional interface), locality (an encapsulating capability to hide internal details of the model), and expressive power (consistency with commonly used notations) help us evaluate the level of conceptual abstraction.

(2) *Functional completeness.* Functional completeness implies the generality of the smallest partitioned logic components for circuit design. A set of the smallest partitioned logic components with ideal functional completeness is capable of accomplishing any circuit design at any design level.

(3) *Structural regularity.* Structural regularity means consistency and standardization of certain design aspects over manageable design constraints encountered during physical design and fabrication processes. The design strategy for structural regularity captures structural and physical requirements primarily as topological constraints, filters out implementation design rules, and offers regular rules for construction of the circuits. Technically, it answers implementation questions such as the cell-set implementation and cell routing design. The design style shows the external property of structural regularity for a specific design and fabrication process (such as one-dimensional placement in standard-cell design and two-dimensional placement in general cell design).

(4) *Design composability.* The structured IC design method allows us to compose circuits topologically onto a two-dimensional grid while simultaneously doing logical design.

Optimal logic partitioning is NP-complete in nature.[1] In practice, the size of the partitioning problem makes it impossible to perform the exhaustive search required to find an optimal partition. The PPL logic partitioning scheme relies on small partitioning granularity and topologically functional orthogonality. It is an approximate yet significantly better solution for the logic partitioning problem.

**Granularity for partitioning.** Several classes of partitioning strategies have been used to implement a structured framework into a CAD system. (Some of these strategies appear in *Physical Design Automation of VLSI Systems*, B.T. Preas and M. Lorenzetti, editors.[1]) We can roughly classify them into low-level partitioning schemes, at the primitive symbolic and stick-diagram level, or high-level partitioning schemes, at or beyond the functional cell and macro level.

A CAD system implemented with lower level partitioning generates circuit layout for each primitive symbol (a via, a wire, etc.) at the physical layout level in terms of a given set of technology specifications. This kind of design system must manage numerous classes of information where each class is associated with a tremendous amount of data. Conversely, a CAD system implemented with high-level partitioning generates macros that are usually inappropriate for the particular application, space-inefficient, and inflexible.

A representative example of a CAD system with a high-level partitioning scheme is the standard-cell design method, which generates circuit cells and macros at or above certain logic functional levels. However, functional macros representing the higher level circuits lack the generality for versatile, area-efficient circuit design. They can only construct a circuit at or above the level at which the macro was designed. Each minor modification in the macro circuit schematic design, or in its physical layout, requires the regeneration of a completely new, full-custom macro. Therefore, it is not unusual to see a typical standard cell library containing several hundred complex cells to accomplish most circuit designs. The standard-cell library usually has a standard-cell module generator for generating the rest of the necessary cells.

In short, our experience has shown partitioning granule size to be a dominant factor in determining an optimal partitioning (in terms of abstraction, functional completeness, structural regularity, and universal composability in circuit design). The lower level fine-granule partitioning scheme possesses a high degree of functional completeness, but lacks abstraction power for low-level physical details. This partitioning scheme loses structural regularity and greatly increases computation overhead. In contrast, the higher level coarse-granule partitioning scheme possesses excessive high-level abstraction power (one symbol could represent hundreds of logic components), but lacks functional completeness. Therefore, it loses design generality and composability, resulting in an inordinate amount of effort to redesign new macros.

A structured VLSI design strategy such as PPL offers an attractive engineering method using a low-level small-granule partitioning scheme. The logic-partitioning granule size in the PPL method differs considerably from the fine-granule and coarse-granule sizes of conventional cell-based design. Each simple logic partition in the PPL method is chosen to perform a simple logic function. The simplest and most general logic functions should include

- Signal passing. This logic function indicates a signal interconnection where a logic value input into and output from this partitioned logic component remain unchanged.
- Signal inversion. The PPL design is based on a distributed logic system made up of a plane of AND gates interleaved with a plane of OR gates. Two important characteristics mark this design approach. First, each logic variable of a vertical column bus can act as a binary variable or perform a logical OR function of the row inputs. When the column segment represents a variable, the values can be set and reset by the row's logic variable value. Second, each logic value of a row bus is a conjunction or product term over the selected column variables; a column input may be either the column value or its complement, or there may be no connections from the column to that row. These variables are ANDed to form the row value. In a more general sense, these logic functions can be viewed as signal inversion for different permutations of input and output over vertical and horizontal signal buses. They can be implemented by a single transistor (in NMOS or GaAs) or a pair of complementary transistors (in CMOS).
- Active loads. In NMOS and GaAs designs, active resistors are used for loading the inverter output. This function can also be implemented using a single transistor.

In Figure 16, an NMOS inverter could be partitioned into two simple logic partitions, a pullup component and a single inversion transistor. They are assigned explicit symbolic representations, "t" (transistor) and "p" (pullup).

The small partitioning granule (based on a single transistor in NMOS or GaAs or a pair of complementary transistors in CMOS) of the PPL method has several advantages:

(1) Each partitioned logic component has a symbol assigned to it. Manipulation of symbols rather than circuits gives a level of abstraction that improves our ability to partition a circuit.

(2) To generalize a design method for a wide range of IC designs, a logic partitioning scheme that allows the decomposition of the circuit logic into its simplest and most general components is appropriate. The simpler each partitioned logic component is, the more general is the logic function associated with this logic component. Since the PPL logic partitioning scheme is based on a single transistor (in NMOS or GaAs) or a pair of complementary transistors (in CMOS), it is capable of building VLSI circuits at any level.

A partition set with a collection of the smallest and simplest logic partitions permits effective circuit design at many design levels, ranging from the transistor level to the gate level, macro level, circuit level, and system architecture level. Structured CAD systems that do not use simple logic partitioning schemes cannot implement an IC at all of these arbitrary design levels.

In PPL logic partitioning, a few simple logic functions represent a high degree of functional completeness for general circuit design.

(3) Structural regularity can easily be implemented using collections of simple PPL cells. These collections of cells can be physically arranged to fit in a regular structure.

(4) Once these simple logic components are implemented, you have achieved universal design composability.

**Topologically functional orthogonality.** Small partitioning granularity provides solutions to conceptual abstraction and functional completeness. For example, the two simple logic partitions in Figure 16, "p" and "t," are functionally complete with definite symbolic meaning — they can be used to form NOR gates. Each logic partition, however, represents an abstract symbol for a logic schematic. This symbol can then be associated with a spatial representation for a two-dimensional VLSI chip implementation. To relate an abstract symbol with an individual layout area which can further be constructed in terms of given topological constraints (the VLSI fabrication technology), functional independence of the partitioned logical components must be reexamined in terms of the (VLSI layout) topological constraints. For simplicity, we have based the following discussion about topologically functional orthogonality on NMOS technology.

If we assume a simple connection network consisting of three visible interconnection wires (horizontal row wire *Row*, left vertical column wire *Lcol*, and right vertical column wire *Rcol*) and two hidden power supply wires (Gnd and Vdd) as shown in Figure 17, each of these wires is built into each small logic component. Any two of the three visible wires could serve as the input and output of the inverter.

Topologically, an inverter that gets an input signal from Row differs from one that gets input from Lcol, although they share similar logic schematics. Therefore, to maintain topologically functional orthogonality, topological constraints (such as interconnection) are enforced over the set of partitioned logic components. Thus, we can produce a set of topologically orthogonal logic components from these two cells. For example, a pullup component, "p," has three topologically orthogonal embodiments, and an inversion transistor, "t," has six topologically orthogonal embodiments, as illustrated in Figure 17 (*m* is a topological modifier number for "p" and "t"). The topologically orthogonal logic partitions in Figure 17 enable you to design an inverter in any arbitrarily horizontal or vertical direction, using any connection as the input or output (see Figure 18).

This topologically functional orthogonality produces the following desirable features in the small partitioning granule:

(1) The small-granule partitioning scheme abstracts the partitioned logical component at a symbolic level. Topologically functional orthogonality provides further abstraction of those components' distinct topological structures.

(2) The few simple logic functions identified in the PPL small-granule partitioning scheme described here are functionally complete. By obeying topological functionality, we can produce a set of partitioned logic components able to meet many structural constraints. Our past research indicates that approximately 15 to 20 of these small, simple PPL logic cells suffice for construction of a general two-dimensional IC layout. This requires a minimal effort when updating a new VLSI technology into an existing CAD system.

(3) Structural regularity (including two-dimensional placement, four-sided local routing and global communication, etc.) can easily be designed and implemented for various given structural constraints and technologies.

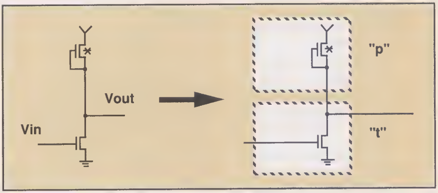

Figure 16. NMOS inverter.

Partitioning with topologically functional orthogonality produces distributed logic components. Each implements a two-dimensional, topologically distributed logic function. The distributed logic function can be specified by *function(symbol, x-coordinate, y-coordinate)*. This additional functional regularity reduces the need for large computing resources, required in circuit database management, topological circuit extraction, and topological circuit simulation.

(4) The small-granule partitioning scheme and topologically functional orthogonality together contribute to a flexible composability for building ICs. The former defines implicit generality for circuit design; the latter, as shown in Figure 18, implements explicit design composability. For example, if we place one pullup and one transistor in two neighboring positions, we can construct a total of 12 different inverter configurations, each with a four-sided routing pattern. Meanwhile, all connection wires in those two components can be used as input, output, and bidirec-

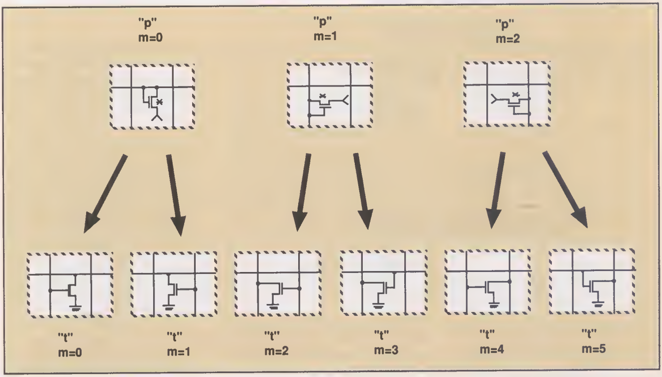

Figure 17. Topologically orthogonal components for "t" and "p" (NMOS).

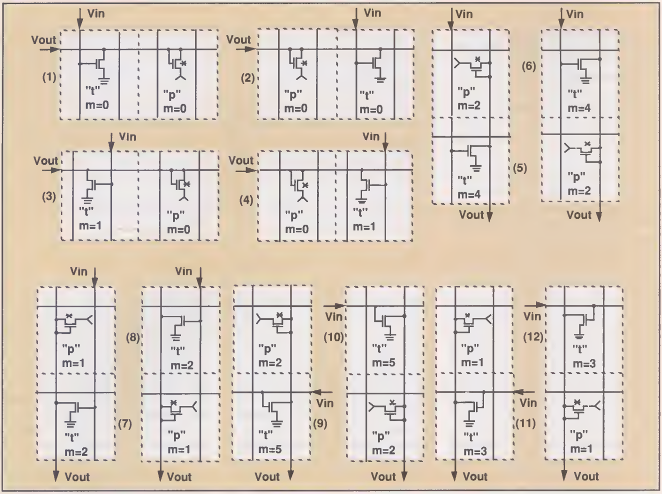

Figure 18. Various structural representations of an inverter (NMOS).

tional communication buses. Compared to other cell-based structured designs, this provides a significantly higher degree of flexibility.

## The PPL tools

The PPL design system (composed of the PPL design tools) is a specific embodiment of the PPL design method. The PPL system includes three software packages used alternatively in the design process: a structured logic editor, Tiler[10]; a PPL circuit extractor, Simpplex[11]; and a unit delay simulator, Simppl.[11]

Tiler is a special interactive editor used for designing VLSI circuits. You insert PPL cells (*tiles*) into a rectangular grid by typing characters representing the cells. When you first start Tiler, it prompts you for the technology to use in designing a PPL circuit. When you give a technology name, a technology file is loaded into Tiler.

Simpplex is a PPL circuit extractor (with electrical rules check). The output of Simpplex is fed into a PPL circuit simulator.

Simppl is a switch-level simulator designed for simulating circuits built using the PPL method. In addition to using a switch-level model, Simppl uses multiple logic values (six for MOS) to model the operation of soft and hard nodes, buses, wired logic, and dynamic logic. It provides both soft and hard values for the true and false logic levels. Since placing PPL symbols on the entire plane automatically defines the complete circuit schematics, simulation by Simppl does not require the extraction of circuit schematics.

The PPL tools have the following features:

- All user interaction occurs through a conventional CRT terminal connected to a mainframe or personal computer. This means that we do not require costly graphics systems or special VLSI design workstations.
- The circuit is represented as an array of the PPL symbols. In this representation, the locations within the array correspond to actual physical locations in the fabricated ICs. Thus, the editor gives you simultaneous perception of both the circuit's logic function and its topological appearance.
- Tiler's user interface resembles a high-level, screen-oriented text editor, such as Emacs. Tiler allows cursor movement and scrolling in any of four directions and supports many helpful editing commands, including replication of, deletion of, and relocation of a single PPL cell or a large collection of PPL cells. Tiler gives you a full-screen view into the complete PPL design, allowing easy movement through the entire IC circuit design.
- The use of symbols within the editor makes it possible to do many high-level operations involving symbol manipulation and pattern recognition that are not feasible in conventional IC design systems. These operations include the enforcement

of topologically and electrically required placement restrictions (illegal adjacencies of cells and illegal placement locations, stipulated by shared wires and cell mirroring), and the automatic placement of connections between physically adjacent cells.

## Practical assessment of the PPL design method

The efficiency and effectiveness of the PPL design method can best be evaluated in three important and complementary ways:

(1) by comparing the design time and circuit density of the circuits implemented using PPL and other custom and semicustom circuit design techniques;
(2) by demonstrating the functionality and execution speeds of actual fabricated circuits designed using the PPL method; and
(3) by investigating PPL's educational impact on training inexperienced students for IC design.

Although some statistical data has been accumulated during the past several years, clearly a comprehensive evaluation in terms of the above criteria could be time-consuming and very expensive. However, the data given below offer a justifiable background for evaluation of the PPL method.

**Comparison with other custom and semicustom design methods.** In all of the following examples, design time measures the time from the inception of the project to the submission of the circuit for processing.

*Example 1.* During March 1988, three Japanese electrical engineers from Okidata Inc. came to discuss the PPL design method at the University of Utah. Rentek Inc., a company located in Salt Lake City, implemented an existing Okidata circuit — originally designed by Okidata using full custom layout methods — with PPL. Designing the new chip using PPL took about three to four person-weeks. The finished chip measured approximately half the size of the original full-custom chip, which took the Okidata engineers approximately one person-year to implement.

*Example 2.* During the spring of 1988, the VLSI Group at the University of Utah implemented a Haugenhauer filter using PPL methods and CAD tools. This filter was initially designed by an agency of the federal government using conventional techniques, including standard cells and a silicon compiler. These designs (i.e., the standard cells and the silicon compiler) resulted in chips approximately three times as large as that of the PPL design. The PPL circuit design took a few person-weeks compared to the several months required for the conventional design.

Figure 19 shows two comparisons in terms of design time and density of the circuits designed using PPL and other circuit design methodologies. Rentek collected the data during its VLSI circuit designs. Figure 20 shows a detailed design time comparison of ICs designed using full-custom, gate-array, and PPL methods. Rentek collected the data independently.

**Performance of ICs designed with PPL.** The following examples give some real-chip performances for NMOS, CMOS, and GaAs ICs designed using the PPL method. Our research efforts in recent years have concentrated on CMOS and GaAs only.

*NMOS chip example.* A RISC chip containing several thousand transistors was designed by students at the Technion in Israel using the PPL method for a 4.0-micron NMOS technology. All 12 chips were fabricated, tested, and found to be functionally correct, with clock frequencies of about 4 MHz and power consumption of 0.4 Watts.

*CMOS chip example.* A first-year graduate student at the University of Utah designed and built a real-time signal and image processor. The single-processor chip contained 9,440 transistors and was implemented using PPL methods in approximately eight person-weeks. The MOS Implementation Service (MOSIS), operated by the University of Southern California for the Department of Defense and the National Science Foundation, fabricated the IC using a 3.0-micron CMOS technology. The MOSIS facility fabricated 44 chips and returned them to the University of Utah for testing. Among them, 33 of the chips were fully functional up to 16-MHz (some up to 20-MHz) clock rates.

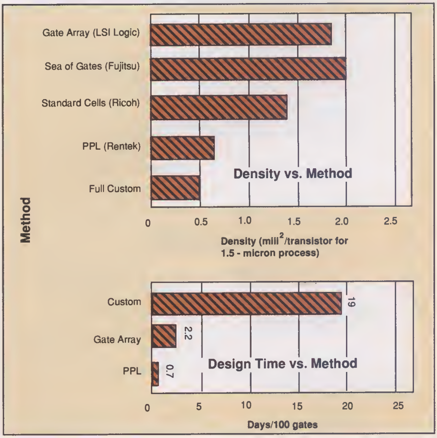

**Figure 19. Comparison of design density and time with different methods (courtesy of Rentek).**

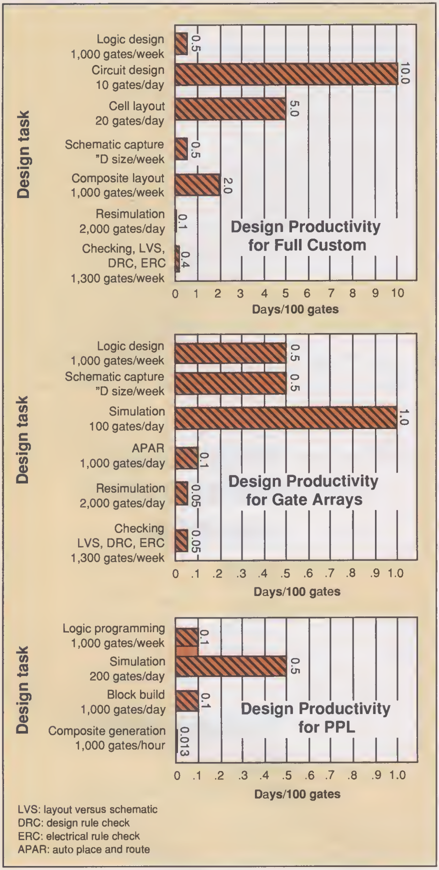

**Figure 20. Detailed comparison of design time with different methods (courtesy of Rentek).**

The complete system, which consists of a cluster of the single-chip processors, was demonstrated for real-scene and medical-image segmentation and processing for video camera images.[12]

*GaAs chip examples.* We fabricated our first GaAs chip designed using PPL in a GaAs multiproject chip. We worked in conjunction with the University of California at Santa Barbara. The actual fabrication took place at Giga Bit Logic in Thousand Oaks, California, using a 1.0-micron GaAs technology. This circuit was tested at the University of Utah and found to be functionally correct.

During collaborative research between the University of Utah VLSI Group and the Unisys Military System Division, Unisys designed 10 complex GaAs circuits using PPL methods. All fabricated circuits worked on the first pass, and the speeds of the circuits fell in the range of 300 MHz to 1 GHz (most fell in the 500-MHz to 1-GHz range).

We have also implemented PPL cell sets for TriQuint and Vitesse GaAs technologies. Recent integration and yield improvements in the Vitesse GaAs foundry at Camarillo, California, should permit us to design PPL GaAs circuits containing approximately 20,000 to 30,000 gates on 7 × 8 mm chips.

**Educational impact of the PPL design method.** Because of its user-friendly and cost-effective nature, PPL lends itself well to VLSI education. By using the PPL tools, students can in a few weeks implement MOS and GaAs ICs containing several thousand to more than 100,000 transistors. Students have successfully designed, had fabricated, and tested numerous application-specific ICs, reduced instruction set computers, microprocessors, and multiprocessors.

These chip design projects cover a wide range of research areas, such as digital signal and digital image processing, computer and multiprocessor networks, digital communication and coding systems, microprocessor and RISC computers, computer arithmetic, fast database machines, CPU and computer resource management, artificial intelligence architectures, computer graphics and computer vision, parallel and distributed computer simulation, and many other applications. Students' direct involvement in VLSI research projects has strongly influenced and contributed to many research programs at the University of Utah sponsored by the

National Science Foundation, Defense Advanced Research Projects Agency, and National Aeronautics and Space Administration.

The VLSI course taught at the University of Utah runs for three consecutive quarters. Two quarters cover background education in ICs. Most of the materials taught are based on a variety of CAD tools generally available at other universities and industrial companies. The third quarter focuses on students' VLSI design projects, based mainly on PPL methods. Projects must be accomplished during the single quarter by one student or a group of several students.

According to the statistics collected over the past seven years, students took an average of 200 person-hours to complete VLSI design projects containing 10,000 to 100,000 transistors. They spent about 20 to 40 hours learning the PPL design method and getting familiar with the PPL design tools. Half of the remaining time (about 80 to 90 hours) went into studying, defining, and designing the project. The rest of the time (another 80 to 90 hours) went for implementation of the VLSI circuits using PPL methods and tools. Most of the circuits fabricated using NMOS, CMOS, or GaAs technologies were later tested and found to be functionally correct.

A large number of the projects have appeared in previous collections of the Utah Annual Student VLSI Design Contest, University of Utah Computer Science Department technical reports, and various publications. We believe that the VLSI course and student projects based on the use of PPL and other VLSI tools make important contributions to education.

A logic partitioning scheme for VLSI based on small-granule partitioning and topologically functional orthogonality possesses a high degree of conceptual abstraction and functional generality and offers excellent structural regularity and design composability. PPL is based on this partitioning scheme.

We have investigated the reasons why PPL methods enable quick and user-friendly implementation of high-performance integrated circuits:

(1) From a design process point of view, conventional IC design separates into roughly three distinct areas: system architecture design, logic design, and composite layout design. Designers in each area are effective only within that specific area. Furthermore, the separation between these areas enforces serious design constraints, resulting in performance penalties. In PPL design, these three areas merge into one step. This gives the designer maximum freedom and the ability to work at any design level within any area.

(2) From a technical point of view, a set of some 15 to 20 simple PPL cells can be implemented in a full-custom design in terms of certain optimal criteria within a short period of time. This would be impossible for standard-cell or full-custom designs requiring hundreds of standard cells or the design of an entire chip.

(3) Compared to semicustom (coarse-granule) methods, the PPL small partitioning granule permits general and less-redundant circuit design, producing area-efficient circuits. Compared to full-custom (fine-granule) design, the PPL symbolic abstraction capability enables quick turnaround time so you can quickly refine different competing circuits to achieve comparable densities.

The PPL design method has some drawbacks. For example, the logic representation in PPL circuit design is distributed topologically through a two-dimensional layout plane (as shown in Figure 9). This could result in hard reading for beginners. As in other VLSI design methods, however, you can always design a circuit using PPL with the distributed logical representation intact.

The structured, symbol-based IC design methods represented by PPL provide significant opportunities for future research and development. Our plans include work in the following areas:

1. Enhanced graphics capability to give simultaneous views of the IC at multiple levels — symbolic, logic, schematic, and composite.
2. Module generators for automatically building PPL representations of such blocks as finite state machines, RAMs, ROMs, arithmetic logic units, counters, etc.
3. Technology-independent design techniques for NMOS, CMOS, and GaAs technologies.
4. Tools and circuits using the PPL method to combine analog and digital IC designs on the same chip.
5. The use of very high density logic to provide functional descriptions directly translatable to PPL circuits.

All of these exciting areas of research have been made possible by the simple, structured approach provided by the PPL method.☐

## Acknowledgments

We extend special thanks to Tony Carter and Ran Ginosar, who are faculty associates at the University of Utah, and to Steve Jacobs and Rick Neff, who are full-time employees in the VLSI Group. Without their significant contributions in the past and their ongoing support, this research would not be possible. We wish to acknowledge students in the VLSI Group for their efforts during the past decade.

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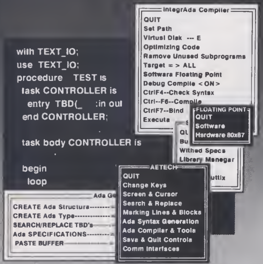

```
with TEXT_IO;
use  TEXT_IO;
procedure   TEST is
 task CONTROLLER is
   entry  TBD(_     :in out
 end CONTROLLER;

 task body CONTROLLER is

 begin
  loop
```

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**Jun Gu** is a PhD candidate in the Department of Electrical Engineering at the University of Utah. Presently, he is a research assistant professor of computer science at the University of Utah and also an assistant professor of electrical engineering at the University of Calgary.

Gu has been involved and actively published in several research areas in artificial intelligence and cognitive science, parallel and distributed processing, computer architecture and its performance evaluation, and intelligent and structured techniques and CAD systems for MOS and GaAs VLSI circuit design. He has twice been awarded ASC fellowships and twice been awarded University of Utah research fellowships. He was twice a recipient of ACM/IEEE academic scholarship awards.

Gu received the BS degree in electrical engineering from the University of Science and Technology of China (USTC) in 1982 and the PhD degree in computer science from the University of Utah in 1989. He is a member of the IEEE, IEEE Computer Society, ACM, International Neural Network Society, and Sigma Xi.

**Kent F. Smith** has served as the chairman of the Department of Computer Science at the University of Utah. He is presently a professor of computer science and research professor of electrical engineering at the University of Utah. He received his PhD from the University of Utah in 1982. He had more than 20 years of experience in the integrated circuit industry prior to joining the faculty at the university. His area of specialization is in the development of CAD tools for the design of structured logic integrated circuits.

Smith has authored more than 46 technical articles and 16 patents. He started the VLSI program at the University of Utah in 1978 and has served as director of the VLSI Group. The group has been involved in many MOS and GaAs VLSI architecture design, implementation, and fabrication projects.

Readers may contact Gu at the University of Calgary, Dept. of Electrical Engineering, 2500 University Dr., NW Calgary, Alberta, Canada T2N 1N4, and Smith at the University of Utah, Computer Science, 3190 Merrill Engineering Building, Room 3190, Salt Lake City, UT 84112.

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*Advance Announcement*

DATA ENGINEERING

# The Sixth International Conference on Data Engineering

February 5-9, 1990
Los Angeles Airport Hilton and Towers
Los Angeles, California

***General Chairperson:** Joseph E. Urban, Arizona State University*
***Program Chairperson:** Ming T. (Mike) Liu, Ohio State University*

## *Scope*

Data Engineering is concerned with the semantics and structuring of data in information systems design, development, management and use. It encompasses both traditional applications and issues, and emerging ones. The purpose of this conference is to provide a forum for the sharing of practical experiences and research advances from an engineering point of view among those interested in automated data and knowledge management We expect that this sharing will enable future information systems to be more efficient and effective, and future research to be more relevant and timely.

**The tutorial titles and schedule:**

- No. 1: *Object-Oriented Database Management Systems*
  Sandra Heiler, Xerox; Stanley Zdonik, Brown University
  Monday, February 5, 8:30 am to 5:00 pm
- No. 2: *Integrating Heterogeneous Distributed Databases: Requirements, Concepts and Solutions*
  Amit P. Sheth, Bellcore
  Monday, February 5, 8:30 am to 5:00 pm
- No. 3: *Relational Database Design Fundamentals*
  Ramez A. Elmasri, Univ. of Houston; Sham B. Navathe, Univ. of Florida
  Monday, February 5, 8:30 am to 5:00 pm
- No. 4: *Deductive Database Systems: An LDL Perspective*
  Ravi Krishnamurthy and Shamim A. Naqvi, MCC
  Monday, February 5, 7:00 pm to 10:15 pm
- No. 5: *Distributed Database Management Systems*
  M. Tamer Ozsu, University of Alberta
  Monday, February 5, 7:00 pm to 10:15 pm
- No. 6: *Spatial Database Systems*
  Oliver Gunther, University of Ulm, West Germany
  Monday, February 5, 7:00 pm to 10:15 pm
- No. 7: *Approaches to Database Security*
  Teresa F. Lunt, SRI International
  Tuesday, February 6, 7:00 pm to 10:15 pm
- No. 8: *Data Replication in Distributed Systems*
  Amr El Abbadi and Abdelsalam Heddaya, Boston University
  Wednesday, February 7, 7:00 pm to 10:15 pm
- No. 9: *Expert Database Systems: A Tutorial*
  Larry Kerschberg, George Mason University
  Part I, Thursday, February 8, 7:00 pm to 10:15 pm
  Part II, Friday, February 9, 8:00 am to 11:30 am
- No. 10: *Optical Database Machines*
  P. Bruce Berra, Syracuse University
  Friday, February 9, 8:00 am to 11:30 am
- No. 11: *Database Management Systems for Software Engineering*
  Gail E. Kaiser, Columbia University
  Friday, February 9, 8:00 am to 11:30 am

## *Invitation*

This conference will prove well worth attending. Dr. Kenneth Wilson, a Nobel laureate in Physics and an expert in supercomputing, will deliver the keynote address at the opening plenary session. There will be three days for the presentation of 66 papers in general sessions and three panels in three tracks. Four full-day and seven half-day tutorials will provide an opportunity for intensive exposure to specific data engineering topics. In addition, time will be available for questions and discussions. Come and join us!

**Conference general sessions and panels will be held on Tuesday, February 6 through Thursday, February 8. Papers and panels related to the following topics will be presented and discussed:**

- Object-Oriented Database Issues
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- Query Languages
- Views and Representations
- Concurrency in Advanced Systems
- Query Languages and Processing
- Panel: Resolving Semantic Heterogeniety
- Distributed Control Algorithms
- Query Processing Techniques
- Object-Oriented Engineering Designs
- Database Operations
- Knowledge Structuring and Modeling
- Replication Management
- Database Security
- Large Knowledge-based Systems
- Update Policies and Propagation
- Panel: Security in Databases
- Integration: Applications and Tools
- Database Structures and Access
- Database Machines
- Extension of Relational Models and Systems
- Files and File Structures
- Database Design Issues
- Transaction Models
- Panel: Issues in Data Engineering

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| Full-day Tutorial | $175.00 | $220.00 | |

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- ☐ Tutorial 2: Integrating Heterogeneous Distributed Databases: Requirements, Concepts and Solutions *(full-day)*
- ☐ Tutorial 3: Relational Database Design Fundamentals *(full-day)*
- ☐ Tutorial 4: Deductive Database Systems: An LDL Perspective *(half-day)*
- ☐ Tutorial 5: Distributed Database Management Systems *(half-day)*
- ☐ Tutorial 6: Spatial Database Systems *(half-day)*
- ☐ Tutorial 7: Approaches to Database Security *(half-day)*
- ☐ Tutorial 8: Data Replication in Distributed Systems *(half-day)*
- ☐ Tutorial 9: Expert Database Sys. *(full-day)*
- ☐ Tutorial 9: Expert Database Sys. Part I *(half-day)*
- ☐ Tutorial 9: Expert Database Sys. Part II *(half-day)*
- ☐ Tutorial 10: Optical Database Machines *(half-day)*
- ☐ Tutorial 11: Database Management Systems for Software Engineering *(half-day)*

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# Synchronous Optical Network and Broadband ISDN Protocols

**Anna Hać and Hasan B. Mutlu**
**AT&T Bell Laboratories**

**The increasing demand for high-performance voice, data, video, and image communication networks has challenged researchers to design some innovative network architectures and protocol and interface structures.**

Future transmission systems will be based heavily on fiber optics technology.[1] Fiber optic networks — the newest technology in data transfer — support the high-speed, low-delay data transfer needed to meet the increasing demand for high-bit-rate applications, particularly image and video services. Fiber optic networks offer not only the speed and capability for tomorrow's network customers, but they also provide the performance demanded for broadband services.

A broadband service requires an information transfer rate exceeding the capacity of a primary-rate interface. Two data rates have been defined for the primary interface: 1.544 megabits per second and 2.048 megabits per second.[2] The interface at 1.544 megabits per second is based on the North American DS-1 transmission structure, which is used for the transmission service. The interface at 2.048 megabits per second, however, is based on the European transmission structure of the same data rate.

The B-ISDN (Broadband Integrated Services Digital Network) is a network that can be used for services requiring high-speed packet switching. It is based on existing ISDN principles, and work to define and standardize B-ISDN is already under way in the International Telegraph and Telephone Consultative Committee (CCITT).[3] The proposed B-ISDN uses a flexible multiplexing format called ATM (asynchronous transfer mode). In the US proposal, Sonet (synchronous optical network) is specified as a physical layer of B-ISDN.[4]

The proposed B-ISDN supports a wide range of audio, video, and data applications in the same network. The service classes of B-ISDN are interactive and distribution services. The interactive services consist of conversational, messaging, and retrieval services involving two-way information exchange between two subscribers. The distribution services are represented by services with and without user individual presentation control. These services include broadcast services and provide a one-way flow of information distributed from a central source to an unlimited number of authorized receivers connected to the network. Examples of broadband services are

- broadband bearer services,
- high-quality broadband video telephony,
- high-quality broadband video conferencing,

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- existing-quality and high-definition TV distribution, and
- broadband videotex.

The primary objective of this article is to provide high-level technical information on Sonet, B-ISDN protocols, and interface structures. Since the B-ISDN protocol standards to be used in the Broadband Reference Model are currently being discussed in the CCITT, most of the standards are not yet available. For example, although CCITT has agreed that ATM will be based on fixed-length cells[1] (a fixed-size packet is called a cell), the length of the cells and the content or length of the cell headers have not been agreed on. Therefore, some of the protocols described here are not based on agreements reached in national and international standards bodies.

## Glossary of acronyms

| | |
|---|---|
| ATM | Asynchronous transfer mode |
| B-ISDN | Broadband Integrated Services Digital Network |
| CCITT | International Telegraph and Telephone Consultative Committee |
| DS-1 | A digital signal in the Bell system digital transmission hierarchy with a specific frame format at 1.544 megabits per second |
| DS-3 | A digital signal in the Bell system digital transmission hierarchy with a specific frame format at 44.736 megabits per second |
| HCS | Header check sequence |
| ISDN | Integrated Services Digital Network — planned foundation for telecommunication service using digital transmission and switching technology to provide voice and data communications |
| ISO | International Standards Organization |
| MAC | Medium access control |
| NNI | Network node interface |
| OA&M | Operation, administration, and maintenance |
| OC-1 | Optical carrier at level 1 |
| OC-*N* | Optical carrier at level *N* |
| OSI | Open Systems Interconnection — a concept that will permit different vendors' products to work together |
| PBX | Private branch exchange — a telephone exchange on the user's premises that provides a circuit-switching capability for telephones on extension lines within the building and access to the public network |
| Sonet | Synchronous optical network |
| STS-1 | Synchronous transport signal at level 1 |
| STS-*N* | Synchronous transport signal at level *N* |
| STS-*Nc* | Concatenated synchronous transport signal at level *Nc* |
| UNI | User network interface |
| VCI | Virtual circuit identifier |

## B-ISDN architecture and ISO model

A computer network can be defined as a collection of host computers that are interconnected (information exchange is possible), autonomous (the computers control themselves), and independently suspicious (they question their input). In any network there are hosts that run application programs. These hosts communicate with each other through the communications subnet. The communications subnet may consist of a set of point-to-point channels connecting switching elements known as nodes, or a single broadcast channel (for example, bus, ring, loop, star, or satellite/radio).

Most networks are designed as a set of layers, each offering a class of transparent services to the layer above. Each layer on a given host establishes a virtual communication with the associated layer on another host. An individual layer within a host receives a message from the next higher level and envelops the message with required information for the corresponding layer in the next host. The expanded message is subsequently passed to the next lower layer. Finally, at the lowest layer, the message is physically transmitted. In the targeted host, each layer strips off the information transmitted by its counterpart and sends the remainder up to the next layer. At the lowest layer, physical communication is established with the corresponding host, but the higher layers use virtual communication.

The set of layers and the associated set of protocols that implement the communication function are called a computer communication architecture. The architecture does not include the interfaces in its definition, since network users have little concern for how a particular system determines its interface structure. The methods for the implementation of a protocol (that is, hardware or software implementation of a specific function) are not characterized by the architecture. As long as correct usage of a protocol is satisfied, the means by which it is implemented does not affect the architecture.

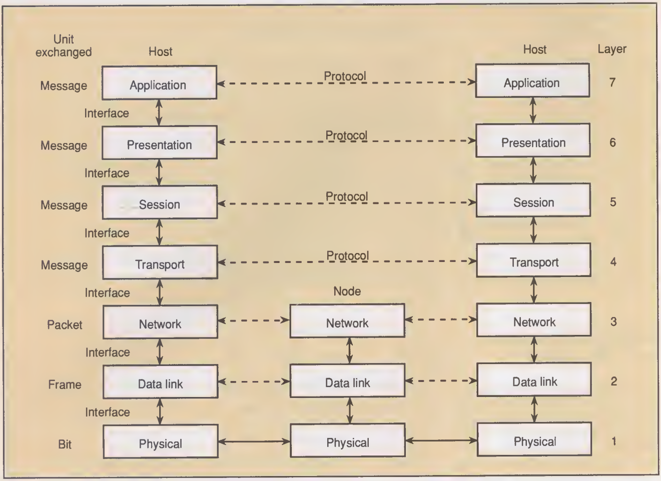

**Figure 1. The International Standards Organization Open Systems Interconnection Reference Model.**

Figure 1 shows a specific layered communications architecture reference model of OSI (Open Systems Interconnection) approved in 1983 as an international standard by both the ISO[5] and the CCITT.[6]

The bottom three layers (1, 2, and 3) of this model provide the networking capability — that is, the agreements between hosts and nodes or between nodes and nodes — and they address issues concerning the communications subnet. (These layers of protocol are called "chained," since the corresponding headers and trailers are removed, tested, and regenerated at every step of the pass across the network.) The upper four layers (4 through 7) administer the processing — at both ends — needed to transmit the information to the end user in a proper and identifiable format. The information associated with these layers is not tested by the nodes. (These layers of protocol are called "end-to-end" protocols.)

This article focuses on the chained layers and defines associated protocols and interface structures to be used by B-ISDN.

## Sonet

In the US proposal to the CCITT, Sonet (synchronous optical network) is recommended as a physical protocol for broadband services. A transmission system for a broadband interface at the physical layer uses framing techniques to transport information. Figure 2 shows the Sonet structure.

Sonet frames allow for both voice channels and broadband services, and they carry framing overhead that is not embedded in the cell structure. Transport overhead is distributed throughout the frame. Each frame consists of 9 bytes of section overhead, 18 bytes of line overhead, 9 bytes of path overhead, and 774 bytes of payload transmitted in a pattern of 3 bytes of section/line overhead followed by 87 bytes of payload plus path overhead. Section overhead is processed at each repeater. Line overhead is passed transparently through repeaters and is processed by terminal equipment at the ends of each span processed by a repeater. Path overhead is passed transparently from the point where the STS-1 (synchronous transport signal at level 1) payload is constructed to the point where it is decomposed. The STS-1 building block consists of transport overhead, path overhead, and the payload. The higher speed STS-*N* (synchronous transport signal at level *N*) is also built of transport overhead, payload, and the path overhead. Transport overhead is replicated in each Sonet STS-*N* frame.

An STS-*N* signal contains *N* copies of the section, line, and path overheads. If an STS-*N* signal is sent between two multiplexers with no intervening demultiplexing, it is permitted to send only one copy of the path overhead. This is an STS-*N* concatenated (STS-*Nc*) signal. Since any intervening transmission equipment ex-

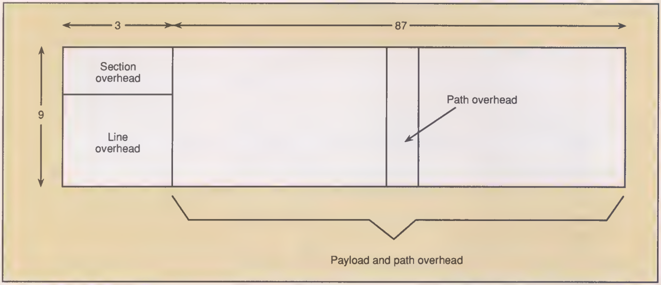

**Figure 2. Sonet structure.**

pects to see the individual section and line overheads embedded in the signal, *N* copies of the section and line overheads are required in the STS-*Nc* signal. For B-ISDN the payload is divided into a number of fixed-length ATM cells, described later.

Broadband interfaces can be framed by using the following techniques (see Figure 3):

(1) A framing pattern is inserted every 125 microseconds (periodic framing, Figure 3a). Customer terminals can derive 125-microsecond timing from the network. Positioned channels based on the 125-microsecond periodic rate can be supported in an ATM-based hybrid interface structure. Synchronous multiplexing is also easier at a higher-than-normal (narrowband) interface rate.

(2) The framing pattern is carried in each cell header (Figure 3b). This allows for lower overhead than in the periodic framing format, if larger cell sizes are selected. An empty cell is not needed to carry the framing pattern. Synchronous multiplexing is also easier at a higher-than-normal (narrowband) interface rate.

(3) Framing overhead is not embedded within the cell structure (Figure 3c). This frame format is used by Sonet, which can carry ATM-based interface structures. When ATM is carried within a Sonet frame, a framing pattern within the cell structure is not required.

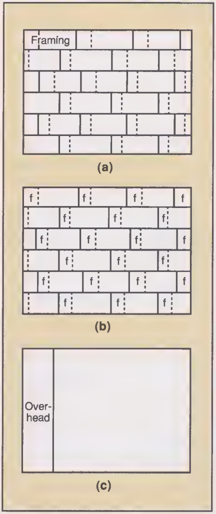

**Figure 3. Formats for framing broadband interfaces: (a) periodic framing, (b) framing pattern in each cell header, (c) no framing in the cell structure.**

Sonet can be used for optical transmission for both the UNI (user network interface) and the NNI (network node interface). At the UNI many of the Sonet overhead bytes are not defined. B-ISDN proposals involving Sonet usually use the STS-3c frame. Sonet bit rates are integer multiples of 51.730 megabits per second. The base bit stream is made up of 125-microsecond frames of 810 bytes, where the bit rate is the integer part of the calculated bit rate. The B-ISDN user network interfaces will use two bit rates: 150 megabits per second and 600 megabits per second. Each of these interfaces will support broadband services and 64-kilobit-per-second-based ISDN services. The US proposes that the 600-megabit-per-second B-ISDN interface be structured either as four byte-interleaved STS-3c signals or as a single STS-12c.[7] Because of the path overhead, the payload of the STS-12c is slightly greater than the payload of four STS-3c signals.

Sonet is based on a layered architecture; Figure 4 shows its hierarchical structure. (The STS-*Nc* is a concatenated synchronous transport signal at level *N*. DS1 and DS3 are the digital signals in the North American digital transmission hierarchy with specific frame formats at 1.544 megabits per second and 44.736 megabits per second, respectively.)

The photonic layer is used for a fiber optic connection of light transfer. The section layer is used for frame transport. The line layer allows for transport of STS-1 through STS-*Nc* blocks between STS-level multiplexers. This layer uses line layer overhead and maps synchronous

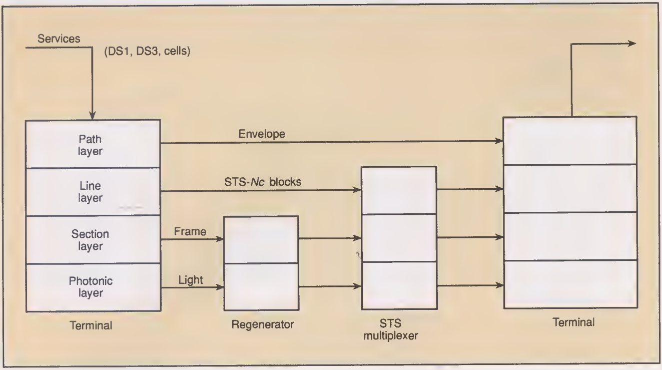

Figure 4. Sonet hierarchical structure.

payload envelopes into a transmission frame. The path layer uses path overhead and maps services into the format of the synchronous payload envelope.

In the US proposals to the CCITT, the B-ISDN transport architecture is based on the Sonet protocol.

The interoffice transport network connects service nodes via transport nodes and high-capacity fiber optic links. The links integrate the transport of voice, data, and video.

In the current architecture proposal for B-ISDN, the main components of the B-ISDN interoffice transport architecture are[8]

(1) *Interoffice facilities*. These are composed of single-mode optical fiber using the Sonet transmission format. The rates for interoffice transport are usually OC-M (OC-24 or higher) and could possibly increase to 2.49 gigabits per second (OC-48) or higher. These rates support the $n \times$ 155.52-megabit-per-second B-ISDN interface rate.

(2) *Sonet OC-M lightwave terminal*. The low- and high-speed interfaces are for the 155.52-megabit-per-second and OC-M optical signals, respectively. Line generation and termination functions include framing, synchronization, line and section overhead processing, and conversion of optical and electrical signals.

(3) *Sonet facility restoration switch*. This switch provides facility protection and restoration rates at Sonet OC-M line rates.

(4) *Transport node controller*. This controller provides control and timing functions for each of the transport node components.

## B-ISDN configuration

A functional reference architecture model for the broadband network is a conceptual division of functions that must be performed in transporting information through the network. It is a useful tool for analyzing and comparing various network architecture alternatives. Figure 5 provides a conceptual model for a B-ISDN reference configuration consisting of functional groupings partitioned by reference points *R*, $S_B$, and $T_B$. (Functional groupings are certain finite arrangements of physical equipment or combinations of equipment. Reference points are conceptual points used to separate groups of functions.) The subscript *B* indicates broadband reference points.

The reference points can also be viewed as physical interface units. Each functional grouping has a different set of functions to perform. The TE (terminal equipment) functions, which include the lowest three layers of the OSI Reference Model, are usually performed by digital telephones, data terminals, and integrated workstations. The TE1 functions follow ISDN recommendations. The TE2 functions do not follow ISDN recommendations; they use the TA (terminal adaptor) converter to connect to a broadband network, since these devices run their own protocols and do not have B-ISDN interfaces (for example, IEEE 802.3 Local Area Network).

The *R* reference point is for non-ISDN physical interfaces, which require TAs to convert the protocol of the TE2 to the ATM-supported $S_B/T_B$ interface of the NT (network termination). User equipment complying with ISDN standards can be connected at the $S_B$ and $T_B$ reference points (dependent on the primary versus basic ISDN rate). The $S_B/T_B$ interface is based on ATM and has the same capacity as the $U_B$ (loop interface). The interfaces at these reference points support 64-kilobit-per-second-based ISDN and B-ISDN services.

The NT2 functions are performed by PBXs (private branch exchanges) and terminal controllers. These functions contain local switching between the $S_B$ interfaces, an $S_B$ interface with the $T_B$ interface, multiplexing of several $S_B$ interfaces at layers 2 and 3, and concentration functions. Note that the NT2 functional grouping can be removed from Figure 5 for a specific configuration. In this case a single interface would bring the $S_B$ and $T_B$ reference points together (hybrid interface), and the NT would then perform all routing functions and switching between terminals on the customer premises. The NT can also multiplex several end-user terminals onto the $U_B$ interface.

NT1 functions terminate the transmission line from the central office. The function of this grouping is to provide the physical layer interworking of the $T_B$ and $U_B$ interfaces. Although only one broadband $T_B$ input is supported, multiple $U_B$ interfaces can also be supported to increase reliability. The $U_B$ interface is the designation for the physical interface between the NT and the local exchange. The functions of the NT1 and NT2 are similar for 64-kilobit-per-second-based ISDN and B-ISDN.

## ATM

B-ISDN is based on a new multiplexing architecture called ATM (asynchronous transfer mode), which associates calls with cells by a label in the header.[4] In a labeled channel, data is put into cells prefixed with a header. The header contains at least one VCI (virtual circuit identifier) that identifies the virtual circuit a cell is associated with, and an error detection field. The information field is transported transparently by the ATM layer of the network, and no processing (for example, error control) is performed on the information field at the ATM layer.[3] The ATM provides great flexibility in supporting both continuous and "bursty" traffic streams by integrating services in common switching and transmission facilities.

**Channel rates.** Narrowband channel rates are defined as follows:

- B — 64 kilobits per second
- H0 — 384 kilobits per second (=6B)
- H11 — 1.536 megabits per second (=24B)
- H12 — 1.920 megabits per second (=30B)
- D — 16/64 kilobits per second

Although the broadband channels are yet to be determined by CCITT, video and high-speed data services are identified as principal applications to be taken into account in determining broadband channel rates. Broadband channels refer to virtual channels with appropriate channel bit

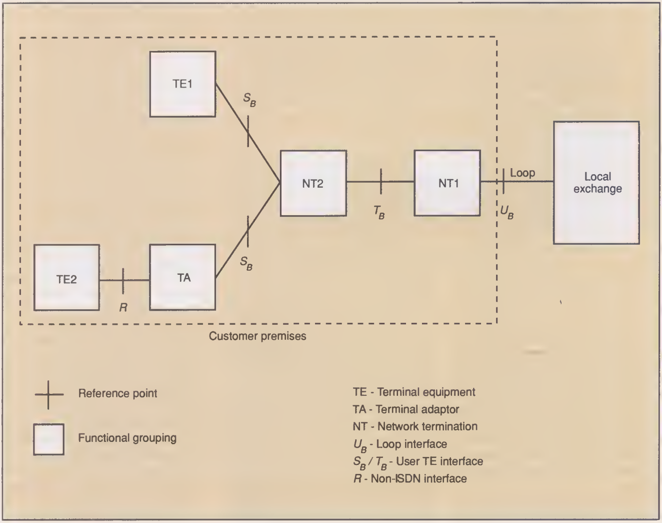

**Figure 5. B-ISDN reference points.**

rates. In addition to B, H0, and H1 narrowband channels, B-ISDN will support broadband channels H2 and H4 with the following bit rates:[3]

- H21 — 32.768 megabits per second
- H22 — 44.160 megabits per second
- H3 — 60-70 megabits per second (not identified)
- H4 — 132.480-138.240 megabits per second (an integer multiple of B channel)

The ATM cell should be designed so that the B-ISDN interface has sufficient payload capacity to carry one H4 channel (for example, applications such as bulk data transfer of text, facsimile, enhanced video information), plus signaling and a small number of narrowband services.[9]

**ATM protocol structure.** The CCITT agreed that B-ISDN will be based on a packetlike ATM structure.[4] Although commercial products using ATM techniques are not currently available, there are a number of experimental implementations.[10]

ATM is the technique for transporting user information within the Sonet payload. Conceptually, the ATM technique can be thought of as a multiplexing scheme in which user information is organized into blocks and each is appended with a header, forming a cell. Multiplexing of the cells onto the Sonet payload is based on the contents of the cell header. Unlike the STM (synchronous transfer mode) technique, which identifies calls by the position of a time slot within a frame, the ATM technique associates calls with cells by a label in the header. This technique also ensures that no bandwidth is consumed by the connection's using a virtual circuit unless information is actually being transported. One advantage of the ATM interface structure is that it can easily carry different types of services with varying data transfer rates. This feature plays an important role in the network integration enhancement process. Because of the dynamic allocation of capacity, the ATM is also sensitive to variations in demand for service and is thus convenient for bursty or continuous data services. Since ATM does not use fixed-rate connections, it can provide higher flexibility in network synchronization.

Although ATM provides many advantages, it also presents several challenges.[11] One is voice delay, since considerable delay could be introduced during creation of the cell. Another challenge is congestion control; momentary overloads could cause buffers in the switches to overflow and cells to be lost.

Figure 6 shows the layers of ATM functions in the ATM protocol model. Two specific layers related to ATM functions are an ATM layer common to all services and providing cell transfer capabilities, and an adaptation layer that is service dependent.[3]

Since the B-ISDN will be used to transfer information from different sources, this information should be adapted into ATM cells to be transported over the B-ISDN network. Transferring information by means of a stream of cells is the basic concept of ATM. The boundary between the ATM layer and the service adaptation layer corresponds to the differences between functions applied to the header and functions applied to the information field. The higher layer functions of the user and control planes and the connections between ATM and non-ATM interfaces are supported by the adaptation layer. Information is mapped by the adaptation layer into ATM cells. At the information transmitting point, the information is divided or collected to be put into ATM cells. At the information receiving point, the information is reassembled or read out from ATM cells. The service adaptation layer can be terminated in NT, TA, and TE.

**ATM cell structure.** The ATM cell structure consists of a header and an information field. Although CCITT has agreed that ATM will be based on fixed-length cells (since they are easier to process at high speeds), the length of the cells and the content or length of the cell headers have not been agreed upon. Currently a header field length of 5 octets and an information field length of 64 octets appear favored in the US. Confirmation of the cell parameters at a header size of 5 octets with an information field of 64 octets is contingent on achieving a mapping into a Sonet STS-3 payload. In addition, voice delay, network delay, header-processing capacity, and transmission efficiency should be studied to determine the exact field size. The header and the information field each consist of a fixed integer number of octets at a given reference point. In addition, the information field length is the same for all connections at all reference points (for example, UNI and NNI) where the ATM technique is applied. According to the recommendation, each ATM cell includes a VCI that associates the information field of the cell with a specific virtual circuit. The Sonet payload available for ATM is 149.760 megabits per second. Usable bandwidth provided by the ATM depends on header and information field size and the manner in which cells are mapped into the Sonet frame.

Figure 7 presents the format of a 5-octet ATM header, which is currently under study.[3] The first octet of the ATM header provides MAC (medium access control) to the physical media, thus providing a contention resolution scheme when multiple terminals are on the same $T_B$ interface. The MAC should be able to support shared access to the media for the B-ISDN services. This first octet can also be used for congestion control. The following two octets and half of the fourth octet include the VCI field, which identifies a particular connection over a UNI or NNI. Although this would allow for more than a million simultaneous connections, only 65,000 simultaneous connections are expected to be used at the UNI. These 65,000 simultaneous connections appear to be adequate and can actually be supported by a 20-bit VCI field.

It is usually assumed that B-ISDN will have the capability to assign some cells priority over other cells. The fourth octet carries the priority-of-information field, which will be consistent for all cells belonging to a call. The priority field includes delay sensitivity and loss sensitivity subfields. This would allow users to determine whether certain cells of a call have higher priority than others. This is useful for multimedia calls or for compressed video calls where sync signals, picture changes, and refresh information could be assigned different priorities. The priority level for a given VCI should remain constant for the duration of the virtual connection to eliminate the possibility of missequencing resulting from a high-priority cell's overtaking a low-priority cell. The fourth octet also includes an OA&M (operation, administration, and maintenance) function to examine the operation of a virtual circuit without interfering with the end user's use of the circuit. Finally, the ATM header includes a field called HCS (header check sequence) to detect and correct errors in the header itself. No detection of errors in the information field is provided at the ATM layer. The fifth octet is used only to detect errors in the header by checking the sum over octets 2, 3, and 4 in the header.

Many European delegations at CCITT recommended using a small cell size (34 octets) with a 2-octet header. The Europeans claim that a larger information field (greater than 32 octets) increases buffering in the network, introduces high voice packetization delay, and causes breakage inefficiencies. However, a longer cell size with larger headers is favored by the majority of delegates.[3]

The important criteria for selection of the ATM information field size are voice delay, efficiency, and cell arrival rate. According to a study conducted by Bell Communications Research, for a typical combination of data services optimum efficiency is satisfied with ATM cells between 50 and 100 octets long, which is much larger than what European administrations propose.[12] Bell Communications Research also demonstrated that to ensure real-time performance, an ATM cell must be processed in the same amount of time it takes to be transmitted.

**Traffic classification for B-ISDN.** The ATM is expected to handle a wide variety of traffic types ranging from circuitlike connections of fixed sized and guaranteed bandwidth to highly bursty data services. Integrating the various traffic types is important for B-ISDN. Therefore, the schemes for packet multiplexing, bandwidth allocation, and congestion control should be investigated to ensure fairness and efficient resource usage. Several studies have already been conducted to address some of the issues of integrating different traffic sources.[13] Although investigating various aspects of traffic integration is beyond the scope of this article, it is important to identify and understand some of the traffic types likely to be integrated in B-ISDN. They may have differences in tolerance to queueing delay, buffering, and bandwidth requirements. Therefore, it is useful to characterize the following B-ISDN traffic types:

(1) *Delay-sensitive high-bandwidth services.* This traffic type requires a fixed high bandwidth for the duration of a call and demands real-time service. Examples of this traffic type are conference video, real-time image and document retrieval, and local area network interconnects.

(2) *Delay-insensitive high-bandwidth services.* This traffic type includes bulk information transport services. The user can designate the extent of delay that is tolerable (specified, for example, as minutes, hours, or overnight). Examples of this traffic type are delay-tolerant document, image, and video delivery services.

(3) *Delay-sensitive low-bandwidth statistically multiplexed services.* This traffic type includes calls that are delay sensitive with end-to-end delay requirements ranging from a few tens to a few hundreds of milliseconds. Examples of such traffic are packetized voice, interactive data, and enquiry-response messages.

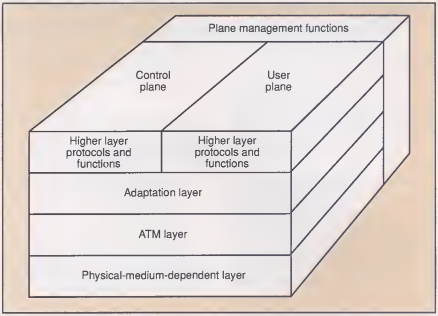
Plane management functions
Control plane
User plane
Higher layer protocols and functions
Higher layer protocols and functions
Adaptation layer
ATM layer
Physical-medium-dependent layer

**Figure 6. B-ISDN asynchronous transfer mode (ATM) protocol model.**

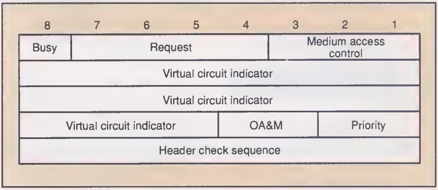
8
7
6
5
4
3
2
1
Busy
Request
Medium access control
Virtual circuit indicator
Virtual circuit indicator
Virtual circuit indicator
OA&M
Priority
Header check sequence

**Figure 7. Asynchronous transfer mode header format.**

B-ISDN is the proposed basis for wide-area networks that will support high-speed, low-delay, functionally rich voice, data, and video applications. ATM is the target information transfer mode solution for broadband networks, and it allows the B-ISDN interfaces to carry thousands of simultaneous data, voice, and video conversations. The US position calls for the interface structures of a broadband interface to be based on ATM and to be built on emerging Sonet-framed interfaces. ATM provides the technology to integrate a wide variety of information into multimedia services by supporting voice, video, and data services separately with varying bandwidth and service requirements. In ATM the information is placed into cells prefixed with a header that includes a label for channel identification.

In the US, Sonet is intended to be the physical layer for B-ISDN. Sonet frames allow for both voice channels and broadband services. The frames carry framing overhead that is not embedded in the cell structure. Transport overhead is distributed throughout the frame. Sonet is based on a layered architecture and can be used for optical transmission for both the UNI and the NNI.

The B-ISDN is based on existing ISDN principles and can evolve by identifying additional functions and services. There is already an increasing demand for high-performance voice, data, video, and image communication networks, and B-ISDN is believed to be capable of meeting these needs once the networks are available and deployed. The B-ISDN protocol standards to be used in the Broadband Reference Model are currently being discussed in the CCITT, and most of the standards are not available yet. Therefore, some of the protocols described here are not based on agreements reached in national and international standards bodies.☐

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**Anna Hać** is a member of the technical staff in the Advanced Software Technology Department at AT&T Bell Laboratories in Naperville, Illinois. She works on performance analysis and design of object-oriented systems, distributed architectures for software-switching applications, and congestion control in computer communication networks. Her research is in system and work-load modeling, performance analysis, reliability, modeling process synchronization mechanisms for distributed systems, distributed file systems, and distributed algorithms. She has published more than 40 papers in archival journals and international conference proceedings.

Hać received MS and PhD degrees in computer science from the Technical University of Warsaw, Poland, in 1977 and 1982, respectively. She has been a visiting scientist at the University of London, a postdoctoral fellow at the University of California at Berkeley, and an assistant professor of computer science at Johns Hopkins University. She is a member of IEEE, ACM, SIGOps, SIGComm, and SIGMetrics.

**Hasan B. Mutlu**, a member of the technical staff in the Computing Technology Department at AT&T Bell Laboratories in Naperville, Illinois, develops analytical models for measuring the performance of computing systems and computer networks. He worked in several research and development groups responsible for modeling and analysis of computing systems and computer networks. He also belongs to a group responsible for identifying and gathering needed information for validation of the developed models. He proposes improvement plans for the analyzed systems and develops objectives, modeling concepts, and plans to evaluate alternative systems and formulate system plans.

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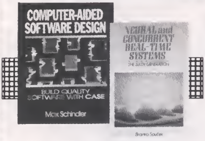
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# Deadlock Detection in Distributed Systems

**Mukesh Singhal**
**Ohio State University**

A distributed system is a network of sites that exchange information with each other by message passing. A site consists of computing and storage facilities and an interface to local users and to a communication network. A primary motivation for using distributed systems is the possibility of resource sharing — a process can request and release resources (local or remote) in an order not known a priori; a process can request some resources while holding others. In such an environment, if the sequence of resource allocation to processes is not controlled, a deadlock may occur.

A deadlock occurs when processes holding some resources request access to resources held by other processes in the same set. The simplest illustration of a deadlock consists of two processes, each holding a different resource in exclusive mode and each requesting an access to resources held by other processes. Unless the deadlock is resolved, all the processes involved are blocked indefinitely. Therefore, a deadlock requires the attention of a process outside those involved in the deadlock for its detection and resolution.

A deadlock is resolved by aborting one or more processes involved in the deadlock and granting the released resources to other processes involved in the deadlock. A process is aborted by withdrawing all its resource requests, restoring its state to an appropriate previous state, relinquishing all the resources it acquired after that state, and restoring all the relinquished resources to their original states. In the simplest case, a process is aborted by starting it afresh and relinquishing all the resources it held.

**Deadlock is a constant problem, often offsetting the advantages of resource sharing. Deadlock handling is difficult in distributed systems because no site has accurate knowledge of the system state.**

**Resource vs. communication deadlock.** Two types of deadlock have been discussed in the literature: resource deadlock and communication deadlock. In resource deadlocks, processes make access to resources (for example, data objects in database systems, buffers in store-and-forward communication networks). A process acquires a resource before accessing it and relinquishes it after using it. A process that requires resources for execution cannot proceed until it has acquired all those resources. A set of processes is resource-deadlocked if each process in the set requests a resource held by another process in the set.

In communication deadlocks, messages are the resources for which processes wait.[1] Reception of a message takes a process out of wait — that is, unblocks it. A set of processes is communication-deadlocked if each process in the set is waiting for a message from another process in the set and no process in the set ever sends a message. In this article we limit our discussion to resource deadlocks in distributed systems.

To present the state of the art of deadlock detection in distributed systems, this article describes a series of deadlock detection techniques based on centralized, hierarchical, and distributed control organizations. The article complements one by Knapp, which discusses deadlock detection in distributed database systems.[2] Knapp emphasizes the underlying theoretical principles of deadlock detection and gives an example of each principle. In contrast, this article examines deadlock detection in distributed systems more from the point of view of its practical implications. It presents an up-to-date and comprehensive survey of deadlock detection algorithms, discusses their merits and

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drawbacks, and compares their performance (delays as well as message complexity). Moreover, this article examines related issues, such as correctness of the algorithms, performance of the algorithms, and deadlock resolution, which require further research.

**Graph-theoretic model of deadlocks.** The state of a system is in general dynamic; that is, system processes continuously acquire and release resources. Characterization of deadlocks requires a representation of the state of process-resource interactions. The state of process-resource interactions is modeled by a bipartite directed graph called a resource allocation graph. Nodes of this graph are processes and resources of a system, and edges of the graph depict assignments or pending requests. A pending request is represented by a request edge directed from the node of a requesting process to the node of the requested resource. A resource assignment is represented by an assignment edge directed from the node of an assigned resource to the node of the process assigned. For example, Figure 1 shows the resource allocation graph for two processes $P_1$ and $P_2$ and two resources $R_1$ and $R_2$, where edges $R_1 \rightarrow P_1$ and $R_2 \rightarrow P_2$ are assignment edges and edges $P_2 \rightarrow R_1$ and $P_1 \rightarrow R_2$ are request edges.

A system is deadlocked if its resource allocation graph contains a directed cycle in which each request edge is followed by an assignment edge. Since the resource allocation graph of Figure 1 contains a directed cycle, processes $P_1$ and $P_2$ are deadlocked. A deadlock can be detected by constructing the resource allocation graph and searching it for cycles.

In a distributed database system (DDBS), the user accesses the data objects of the database by executing transactions. A transaction can be viewed as a process that performs a sequence of reads and writes on data objects. The data objects of a database can be viewed as resources that are acquired (by locking) and released (by unlocking) by transactions. In DDBS literature the resource allocation graph is referred to as a transaction-wait-for (TWF) graph.[3] In a TWF graph, nodes are transactions and there is a directed edge from node $T_1$ to node $T_2$ if $T_1$ is blocked and must wait for $T_2$ to release some data object. A system is deadlocked if and only if there is a directed cycle in its TWF graph. Since both graphs denote the state of process-resource interaction, we will collectively refer to them as state graphs.

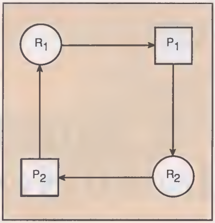

**Figure 1. Resource allocation graph.**

## Deadlock-handling strategies

The three strategies for handling deadlocks are deadlock prevention, deadlock avoidance, and deadlock detection. In deadlock prevention, resources are granted to requesting processes in such a way that a request for a resource never leads to a deadlock. The simplest way to prevent a deadlock is to acquire all the needed resources before a process starts executing. In another method of deadlock prevention, a blocked process releases the resources requested by an active process.

In deadlock avoidance strategy, a resource is granted to a process only if the resulting state is safe. (A state is safe if there is at least one execution sequence that allows all processes to run to completion.) Finally, in deadlock detection strategy, resources are granted to a process without any check. Periodically (or whenever a request for a resource has to wait) the status of resource allocation and pending requests is examined to determine if a set of processes is deadlocked. This examination is performed by a deadlock detection algorithm. If a deadlock is discovered, the system recovers from it by aborting one or more deadlocked processes.

The suitability of a deadlock-handling strategy greatly depends on the application. Both deadlock prevention and deadlock avoidance are conservative, overly cautious strategies. They are preferred if deadlocks are frequent or if the occurrence of a deadlock is highly undesirable. In contrast, deadlock detection is a lazy, optimistic strategy, which grants a resource to a request if the resource is available, hoping that this will not lead to a deadlock.

Deadlock handling is complicated in distributed systems because no site has accurate knowledge of the current state of the system and because every intersite communication involves a finite and unpredictable delay. Next, we examine the complexity and practicality of the three deadlock-handling approaches in distributed systems.

**Deadlock prevention.** Deadlock prevention is commonly achieved either by having a process acquire all the needed resources simultaneously before it begins executing or by preempting a process that holds the needed resource. In the former method, a process requests (or releases) a remote resource by sending a request message (or release message) to the site where the resource is located. This method has the following drawbacks:

(1) It is inefficient because it decreases system concurrency.

(2) A set of processes may get deadlocked in the resource-acquiring phase. For example, suppose process $P_1$ at site $S_1$ and process $P_2$ at site $S_2$ simultaneously request two resources $R_3$ and $R_4$ located at sites $S_3$ and $S_4$, respectively. It may happen that $S_3$ grants $R_3$ to $P_1$ and $S_4$ grants $R_4$ to $P_2$, resulting in a deadlock. This problem can be handled by forcing processes to acquire needed resources one by one, but that approach is highly inefficient and impractical.

(3) In many systems future resource requirements are unpredictable (not known a priori).

In the latter method, an active process forces a blocked process, which holds the needed resource, to abort. This method is inefficient because several processes may be aborted without any deadlock.

**Deadlock avoidance.** For deadlock avoidance in distributed systems, a resource is granted to a process if the resulting global system state is safe (the global state includes all the processes and resources of the distributed system). The following problems make deadlock avoidance impractical in distributed systems:

(1) Because every site has to keep track of the global state of the system, huge storage capacity and extensive communication ability are necessary.

(2) The process of checking for a safe global state must be mutually exclusive. Otherwise, if several sites concurrently perform checks for a safe global state (each site for a different resource request), they

may all find the state safe but the net global state may not be safe. This restriction severely limits the concurrency and throughput of the system.

(3) Due to the large numbers of processes and resources, checking for safe states is computationally expensive.

**Deadlock detection.** Deadlock detection requires examination of process-resource interactions for the presence of cyclic wait. In distributed systems deadlock detection has two advantages:

(1) Once a cycle is formed in the state graph, it persists until it is detected and broken.

(2) Cycle detection can proceed concurrently with the normal activities of a system; therefore, it does not have a serious effect on system throughput.

For these reasons the literature on deadlock handling in distributed systems is highly biased toward deadlock detection.

## Issues in deadlock detection

Deadlock detection involves two basic tasks: maintenance of the state graph and search of the state graph for the presence of cycles. Because in distributed systems a cycle may involve several sites, the search for cycles greatly depends on how the system state graph is represented across the system.

Classified according to the way state graph information is maintained and the search for cycles is carried out, the three types of algorithms for deadlock detection in distributed systems are centralized, distributed, and hierarchical algorithms. In centralized algorithms the state graph is maintained at a single designated site, which has the sole responsibility of updating it and searching it for cycles. In distributed algorithms the state graph is distributed over many sites of the system, and a cycle may span state graphs located at several sites, making distributed processing necessary to detect it. In centralized algorithms the global state of the system is known and deadlock detection is simple. In distributed algorithms the problem of deadlock detection is more complex because no site may have accurate knowledge of the system state.[4] In hierarchical algorithms sites are arranged in a hierarchy, and a site detects deadlocks involving only its descendant sites. Hierarchical algorithms exploit access patterns local to a cluster of sites to efficiently detect deadlocks.

**Correctness of deadlock detection algorithms.** To be correct, a deadlock detection algorithm must satisfy two criteria:

(1) No undetected deadlocks: the algorithm must detect all existing deadlocks in finite time.

(2) No false deadlocks: the algorithm should not report nonexistent deadlocks.

In distributed systems where there is no global memory and communication occurs solely by messages, it is difficult to design a correct deadlock detection algorithm because sites may receive out-of-date and inconsistent state graphs of the system. As a result, sites may detect a cycle that never existed but whose different segments existed in the system at different times. That is why many deadlock detection algorithms reported in the literature are incorrect.

**Strengths and weaknesses of centralized algorithms.** In centralized deadlock detection algorithms, a designated site, often called the control site, has the responsibility of constructing the global state graph and searching it for cycles. The control site may maintain the global state graph all the time, or it may build it whenever deadlock detection is to be carried out by soliciting the local state graph from every site. Centralized algorithms are conceptually simple and are easy to implement. Deadlock resolution is simple in these algorithms — the control site has the complete information about the deadlock cycle, and it can optimally resolve the deadlock.

However, because control is centralized at a single site, centralized deadlock detection algorithms have a single point of failure. Communication links near the control site are likely to be congested because the control site receives state graph information from all the other sites. Also, the message traffic generated by deadlock detection activity is independent of the rate of deadlock formation and the structure of deadlock cycles.

**Strengths and weaknesses of distributed algorithms.** In distributed deadlock detection algorithms, the responsibility of detecting a global deadlock is shared equally among the sites. The global state graph is spread over many sites, and several sites participate in the detection of a global cycle. Unlike centralized algorithms, distributed algorithms are not vulnerable to a single point of failure, and no site is swamped with deadlock detection activity. Deadlock detection is initiated only if a waiting process is suspected to be part of a deadlock cycle.

But deadlock resolution is often cumbersome in distributed deadlock detection algorithms because several sites may detect the same deadlock and may not be aware of other sites and/or processes involved in the deadlock. Distributed algorithms are difficult to design because sites may collectively report the existence of a global cycle after seeing its segments at different instants (though all the segments never existed simultaneously) due to the system's lack of globally shared memory. Also, proof of correctness is difficult for these algorithms.

**Strengths and weaknesses of hierarchical algorithms.** In hierarchical deadlock detection algorithms, sites are arranged hierarchically, and a site detects deadlocks involving only its descendant sites. To efficiently detect deadlocks, hierarchical algorithms exploit access patterns local to a cluster of sites. They tend to get the best of both worlds: they have no single point of failure (as centralized algorithms have), and a site is not bogged down by deadlock detection activities that it is not concerned with (as sometimes happens in distributed algorithms). For efficiency, most deadlocks should be localized to as few clusters as possible; the objective of hierarchical algorithms will be defeated if most deadlocks span several clusters.

Next, we describe a series of centralized, distributed, and hierarchical deadlock detection algorithms. We discuss the basic idea behind their operations, compare them with each other, and discuss their pros and cons. We also summarize the performance of these algorithms in terms of message traffic, message size, and delay in detecting a deadlock (see Table 1). It is not possible to enumerate these performance measures with high accuracy for many deadlock detection algorithms for the following reasons: the random nature of the TWF graph topology, the invocation of deadlock detection activities even though there is no deadlock, and the initiation of deadlock detection by several processes in a deadlock cycle. Therefore, for most algorithms we have given performance bounds rather than exact numbers (for example, the maximum number of messages transferred to detect a global cycle).

**Table 1. Performance comparison of distributed deadlock detection algorithms.**

| Algorithm | Number of Messages | Delay | Message Size |
|---|---|---|---|
| Goldman | $<m.n$ | $\tau + nT$ | Variable (medium) |
| Isloor-Marsland | $r(N-1)$ | 0 | Constant (small) |
| Menasce-Muntz | $m(n-1)$ | $nT$ | Variable (small) |
| Obermarck | $m(n-1)/2$ | $nT$ | Variable (medium) |
| Chandy et al. | $<m.n$ | $\tau + nT$ | Constant (small) |
| Haas-Mohan | $m(n-1)$ | $\tau + (n-1)T$ | Variable (medium) |
| Sugihara et al. | $<m.n$ | $(n-1)T$ | Constant (small) |
| Sinha-Natarajan | best confi. $2(n-1)$<br>worst confi. $m(n-1)$ | $2(n-1)T$ | Constant (small) |
| Mitchell-Merritt | $m(n-1)$ | $(n-1)T$ | Constant (small) |
| Bracha-Toueg | $4m(N-1)$ | $4dT$ | Variable (medium) |

$N$: number of sites; $n$: number of sites in deadlock cycle;
$m$: number of processes involved in deadlock;
T: intersite communication delays;
$\tau$: deadlock initiation delay;
$r$: TWF graph update rate; $d$: diameter of TWF graph

## Centralized deadlock detection algorithms

In the simplest centralized deadlock detection algorithm, a designated site called the control site maintains the state graph of the entire system and checks it for the existence of deadlock cycles. All sites request or release resources (even local resources) by sending "request resource" or "release resource" messages to the control site. When the control site receives such a message, it correspondingly updates its state graph. This algorithm is conceptually simple and easy to implement. However, it is highly inefficient because all the resource acquisition and release requests must go through the control site, causing large delays in response to user requests, large communication overhead, and congestion of communication links near the control site. Also, the algorithm's reliability is poor because if the control site fails, not only does deadlock detection stop, but also the entire system comes to a halt. This is because all the status information resides at the control site.

Some problems of this algorithm (such as long response time and congested communication links near the control site) can be mitigated by having each site maintain its resource status (state graph) locally and by having every site send its resource status to a designated site periodically for construction of the global state graph (and detection of deadlocks). However, due to the inherent communication delay and the lack of perfectly synchronized clocks in distributed systems, the designated site may get an inconsistent view of the system and detect false deadlocks.[5]

For example, suppose two resources $R_1$ and $R_2$ are stored at sites $S_1$ and $S_2$, respectively. Suppose the following two transactions $T_1$ and $T_2$ are started almost simultaneously at sites $S_3$ and $S_4$, respectively:

| $T_1$ | $T_2$ |
|---|---|
| Lock $R_1$ | Lock $R_1$ |
| Unlock $R_1$ | Unlock $R_1$ |
| Lock $R_2$ | Lock $R_2$ |
| Unlock $R_2$ | Unlock $R_2$ |

Suppose the Lock $R_1$ request of $T_1$ arrives at $S_1$ and locks $R_1$, followed by the Lock $R_1$ request of $T_2$, which waits at $S_1$. At this point $S_1$ reports its status, $T_2 \rightarrow T_1$, to the designated site. Suppose the Lock $R_2$ request of $T_2$ arrives at $S_2$ and locks $R_2$, followed by the Lock $R_2$ request of $T_1$, which waits at $S_2$. At this point $S_2$ reports its status, $T_1 \rightarrow T_2$, to the designated site, which, after constructing the global state graph, reports a false deadlock $T_1 \rightarrow T_2 \rightarrow T_1$.

**Ho-Ramamoorthy algorithm.** In an attempt to solve the problem of the above algorithm, Ho and Ramamoorthy have presented two centralized deadlock detection algorithms called the two-phase and one-phase algorithms.[5] These algorithms, respectively, collect two consecutive status reports and keep two status tables at each site to ensure that the control site gets a consistent view of the system.

*Two-phase algorithm.* Every site maintains a status table, which contains the status of all processes initiated at that site. The status of a process includes all resources locked and all resources being waited for. Periodically, a designated site requests the status table from all sites, constructs a state graph from the received information, and searches it for cycles. If there is no cycle, then the system is not deadlocked. Otherwise, the designated site again requests status tables from all the sites and again constructs a state graph, using only the transactions common to both reports. If the same cycle is detected again, the system is declared deadlocked.

Ho and Ramamoorthy claimed that by selecting the transactions common to two consecutive reports, the designated site gets a consistent view of the system (a view that correctly reflects the state of the system) because if a deadlock exists, the same wait-for condition must exist in both reports. However, this claim is incorrect — a cycle in the wait-for conditions of the transactions common to two consecutive reports does not imply a deadlock — and the two-phase algorithm can report false deadlocks. By getting two consecutive reports, the designated site reduces but does not eliminate the probability of getting an inconsistent view.

*One-phase algorithm.* The one-phase algorithm requires only one phase of status reports from sites, but each site maintains two status tables: a resource status table and a process status table. The resource status table keeps track of the transactions that have locked or are waiting for resources stored at that site. The process status table keeps track of the resources locked by or waited for by all the transactions at that site. Periodically, a designated site requests both tables from all other sites, constructs a state graph using only the transactions for which the resource table matches the process table, and searches it for cycles. If no cycle is found, then the system is not deadlocked; otherwise, a deadlock has been detected.

The algorithm does not detect false deadlocks because it eliminates inconsistency in state information by using only the information common to both tables. For example, if the resource table at $S_1$ indicates that resource $R_1$ is being waited for by a process $P_2$ (i.e., $R_1 \leftarrow P_2$) and the process table at $S_2$ indicates that process $P_2$ is waiting for resource $R_1$ (i.e., $P_2 \rightarrow R_1$), then edge $P_2 \rightarrow R_1$ in the constructed state graph correctly reflects the system state. If either of these entries is missing from the resource or process table, then a request message or release message from $S_2$ to $S_1$ is in transit and $P_2 \rightarrow R_1$ cannot be ascertained. The one-phase algorithm is faster and requires fewer messages than the two-phase algorithm. But it requires more storage because every site maintains and exchanges two status tables.

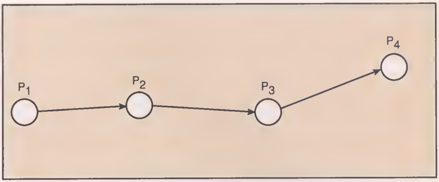

Figure 2. Example of OBPL (ordered blocked process list).

## Distributed deadlock detection algorithms

In distributed algorithms all sites cooperate to detect a cycle in the state graph, which is distributed over several sites of the system. Deadlock detection can be initiated whenever a process is forced to wait, and it can be initiated either by the local site of the process or by the site where the process waits. Information about the state graph can be maintained and circulated in various forms (for example, table,[5] list,[6] string,[7,8] and probe[1,9]) during the deadlock detection phase.

**Goldman's algorithm.** Goldman's algorithm[6] exchanges deadlock-related information in the form of an ordered blocked process list (OBPL), in which each process (except the last) is blocked by its successor. The last process in an OBPL may either be waiting to access a resource or be running. For example, OBPL $P_1$, $P_2$, $P_3$, $P_4$ represents the state graph in Figure 2.

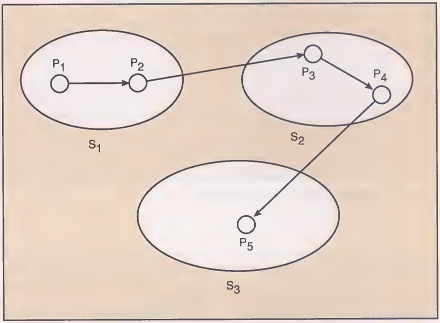

Figure 3. Example of Goldman's algorithm.

The algorithm detects a deadlock by repeatedly expanding the OBPL, appending the process that holds the resource needed by the last process in the list until either a deadlock is discovered (that is, the last process is blocked by a process in the list) or the OBPL is discarded (the last process is running). As an example, suppose in the system shown in Figure 3 process $P_1$ initiates deadlock detection and sends OBPL $P_1$, $P_2$ to process $P_2$. When process $P_2$ receives the OBPL, it appends $P_3$ to the OBPL and sends the new OBPL $P_1$, $P_2$, $P_3$ to $P_3$. Likewise, $P_3$ sends OBPL $P_1$, $P_2$, $P_3$, $P_4$ to $P_4$ and $P_4$ sends OBPL $P_1$, $P_2$, $P_3$, $P_4$, $P_5$ to $P_5$. When $P_5$ receives the OBPL, it discards the OBPL because it is not blocked. Had $P_5$ been blocked by $P_1$, $P_2$, $P_3$, or $P_4$, a deadlock would have been detected by $P_5$.

An advantage of Goldman's algorithm is that it does not require continuous maintenance of TWF graphs. It constructs an OBPL whenever deadlock detection is to be carried out. However, it requires that every process have at most one outstanding resource request.

**Isloor-Marsland algorithm.** The "online" deadlock detection algorithm of Isloor and Marsland[10] detects deadlocks at the earliest possible instant — that is, at the time of making decisions about data allocation at the concerned site. It is based on the concept of reachable set. The reachable set of a node in the state graph is the set of all the nodes that can be reached from it. A process is deadlocked if the reachable set of the corresponding node contains the node itself.

The algorithm detects deadlocks by constructing reachable sets and checking whether any node belongs to its own reachable set. To do this, every site maintains the system state graph and reachable sets for each node in the state graph; the reachable sets are continually updated whenever edges are added to or deleted from the state graph. Whenever a resource is allocated,

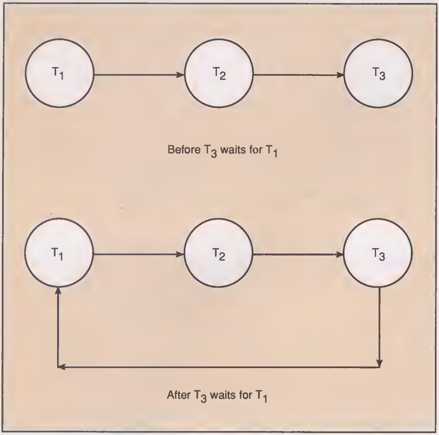

**Figure 4. Example of Menasce-Muntz algorithm.**

whenever a process is made to wait for a resource, or whenever a process releases a resource, the corresponding information is broadcast to all other sites. Therefore, if $r$ changes per second occur in the state graph, then the algorithm requires $r(N\text{-}1)$ messages per second for deadlock detection. However, the messages are short because they contain only an update to the state graph resulting from the execution of a request.

**Menasce-Muntz algorithm.** The deadlock detection algorithm of Menasce and Muntz[3] propagates only the two end points of a directed path (called a blocking pair), rather than the whole path, to detect deadlocks. The blockingset(T) of a transaction T is the set of all nonblocked transactions that can be reached from T by following all directed paths in the TWF graph. This is the set of transactions responsible for blocking the transaction T. When a transaction T gets blocked, then for each transaction $T_i$ in the blockingset(T), the algorithm sends the blocking pair (T, $T_i$) to the home sites of T and $T_i$. (In other words, information about the condensed TWF graph is sent along the paths of the global TWF graph.)

Figure 4 illustrates the algorithm for a deadlock involving three transactions $T_1$, $T_2$, and $T_3$. Initially $T_1$ is blocked by $T_2$ and $T_2$ by $T_3$, and the home sites of $T_1$ and $T_2$ have the knowledge of the TWF graph $T_1 \rightarrow T_2$ and $T_2 \rightarrow T_3$, respectively. Now, when $T_3$ makes a request and is blocked by $T_1$, the blocking pair ($T_3$, $T_2$) is sent to the home site of $T_2$. This causes an edge from $T_3$ to $T_2$ to be added in the TWF of the home site of $T_2$, resulting in a cycle $T_3 \rightarrow T_2 \rightarrow T_3$ and detection of a deadlock at the home site of $T_2$.

Gligor and Shattuck[4] have shown that this algorithm fails to detect some deadlocks for two reasons: First, in the case of a nonlocal request, the determination of whether a transaction is blocked or not is incorrect because that determination cannot be made until the response arrives from a remote site. Second, even if this response arrives to determine correctly whether a transaction is blocked or not, the algorithm does not make use of it. Gligor and Shattuck have fixed this algorithm by precisely defining the status of all the transactions, whether active, blocked, or waiting for the outcome of a nonlocal resource request, and by having the algorithm propagate appropriate blocking pairs when it becomes certain that a waiting transaction is blocked.

**Obermarck's algorithm.** In Obermarck's algorithm,[8] the nonlocal portion of the global TWF graph at a site is abstracted by a distinct node, called "external" or Ex, which helps determine potential multisite deadlocks without requiring a huge global TWF graph to be stored at each site. Deadlock detection at a site follows the following iterative process:

(1) A site waits for deadlock-related information (produced in the previous deadlock detection iteration) from other sites.

(2) The site combines the received information with its local TWF graph, detects all cycles, and breaks only cycles that do not contain the node Ex.

(3) For all cycles Ex$\rightarrow T_1 \rightarrow T_2 \rightarrow$ Ex that contain the node Ex (these cycles are potential candidates for global deadlocks), the site transmits them in string form Ex, $T_1$, $T_2$, Ex to all other sites.

The algorithm reduces message traffic by lexically ordering the nodes (transactions) and sending a string Ex, $T_1$, $T_2$, $T_3$, Ex to other sites only if $T_1$ is higher than $T_3$ in the lexical ordering.

**Chandy-Misra-Haas algorithm.** Chandy, Misra, and Haas's algorithm[1] uses a special message called a probe. A probe is a triplet $(i, j, k)$ denoting that it belongs to a deadlock detection initiated for process $P_i$ and is being sent by the home site of $P_j$ to the home site of $P_k$. A probe message travels along the edges of the global TWF graph, and a deadlock is discovered when a probe message returns to its initiating process. As an example, consider the system shown in Figure 5. If process $P_1$ initiates deadlock detection, it sends probe (1, 3, 4) to the controller $C_2$ at site $S_2$. Since $P_6$ is waiting for $P_8$ and $P_7$ is waiting for $P_{10}$, $C_2$ sends probes (1, 6, 8) and (1, 7, 10) to $C_3$, which in turn sends probe (1, 9, 1) to $C_1$. On receipt of probe (1, 9, 1), $C_1$ declares that $P_1$ is deadlocked.

In Haas and Mohan's algorithm,[7] a variation of Chandy, Misra, and Haas's algorithm, a process comes to know (besides detecting that it is deadlocked) all the deadlock cycles in which it is involved. The algorithm achieves this by passing more information about the potential cycles in a probe message. In this algorithm a message consists of not only the information about the initiator of the deadlock, but also all the paths to it.

**Mitchell-Merritt algorithm.** In the deadlock detection algorithm of Mitchell and Merritt,[11] each node of the TWF graph has two labels: private and public. The private label of each node is unique to that node, and initially both labels have the same value. The algorithm detects a deadlock by propagating the public labels of nodes in a backward direction in the TWF graph. When a transaction gets blocked, the public and private labels of its node in the TWF graph are changed to a value greater than their previous values and greater than the public labels of the blocking transaction. (Blocked transactions update their labels in this manner periodically.) A deadlock is detected when a transaction receives its own public label. In essence, the largest public label propagates in a backward direction in a deadlock cycle. Deadlock resolution is simple in this algorithm because only one process detects a deadlock (that process can resolve the deadlock by aborting itself).

**Sugihara et al.'s algorithm.** As in Obermarck's algorithm, in Sugihara et al.'s algorithm[12] every site maintains only a local TWF graph. A wait for a remote resource is reflected by adding a global edge to the local TWF graphs of the site of the requesting process and the site of the process holding the requested resource. In a global edge the nodes corresponding to the requesting process and the process holding the requested resource are referred to as the O-node and the I-node, respectively (Figure 6).

A site initiates deadlock detection by sending a message, similar to the probe message of Chandy, Misra, and Haas, whenever the addition of an edge (due to a resource wait) in its TWF graph creates a new path between any of its I-nodes and O-nodes. Note that a site can be involved in a global deadlock only when there is a path between some of its I-nodes and O-nodes. The algorithm has a unique resolver for every deadlock, and deadlock resolution does not cause detection of false deadlocks. An advantage of the algorithm is that a site maintains minimal information about the global TWF graph.

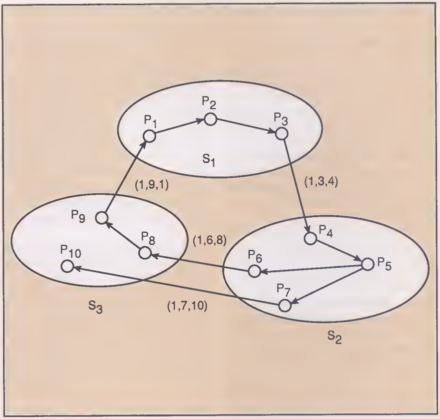

Figure 5. Example of Chandy-Misra-Haas algorithm.

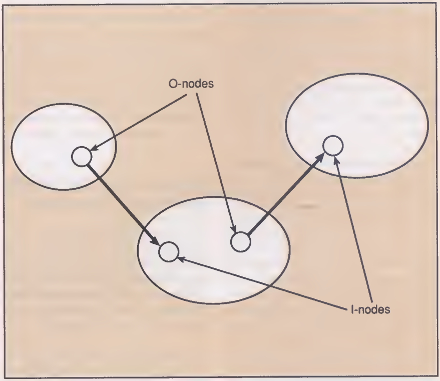

Figure 6. I-nodes and O-nodes.

**Sinha-Natarajan algorithm.** Sinha and Natarajan's algorithm[9] does not construct the TWF graph, but it follows the edges of the graph to search for cycles. Transactions are prioritized, and an antagonistic conflict is said to occur when a transaction waits for a data object that is locked by a lower-priority transaction. The algorithm initiates deadlock detection only when an antagonistic conflict occurs, rather than whenever a transaction begins to wait for another transaction. Therefore, it requires fewer messages to detect deadlocks and generates fewer messages during normal conditions.

The algorithm detects a deadlock by circulating a probe message through a cycle in the global TWF graph. A probe message is a 2-tuple $(i, j)$ where $i$ is the transaction that faced the antagonistic conflict and initiated deadlock detection and $j$ is the transaction of the lowest priority among all the transactions (nodes of the TWF graph) the probe has traversed so far. When a waiting transaction receives a probe initiated by a lower-priority transaction, the probe is discarded. (Thus, the algorithm filters out redundant messages).

An interesting property of this algorithm is that a deadlock is detected when the probe issued by the highest-priority process in the cycle returns to that process. (There is only one detector of every deadlock.) Deadlock resolution is simple; the detector of a deadlock can resolve the deadlock by aborting the lowest-priority transaction of the cycle. Choudhary et al. have shown that this algorithm detects false deadlocks and fails to report all deadlocks because it overlooks the possibility of a transaction waiting transitively on a deadlock cycle and because probes of aborted transactions are not deleted properly.[13]

**Badal's algorithm.** Badal's algorithm[14] exploits the fact that deadlocks can be divided into several categories based on the complexity of their topology; the frequency of deadlock occurrence and the costs of deadlock detection differ among categories. There is no point in detecting simple deadlocks with an algorithm designed to detect complex deadlocks. Badal optimizes performance by using three levels of deadlock detection; activity at each level is more complex (and expensive) than at the preceding level. Deadlock detection starts at the first level algorithm and is delegated to the next higher level if the current-level algorithm fails to report a deadlock. The third-level algorithm is designed to detect global deadlocks that escape the first two levels, and it closely resembles Obermarck's algorithm.

The most attractive feature of Badal's algorithm is that it detects the most frequent deadlocks with minimum overhead (first- and second-level algorithms) and switches to an expensive algorithm (third level) only when really needed. However, it has a fixed overhead due to information kept in lock tables, frequent checking of deadlocks of length two, and longer messages. Consequently, it is most suitable in environments where deadlocks occur frequently, justifying the fixed overhead.

**Bracha-Toueg algorithm.** In Bracha and Toueg's deadlock detection algorithm for generalized environments, called the $r$-out-of-$s$ request model,[15] a process can request any $r$ resources from a pool of $s$ resources. After issuing an $r$-out-of-$s$ request, a process remains blocked until it gets any $r$ out of the $s$ resources. The algorithm consists of two phases: notify and grant. In the first phase, notify messages are propagated downward in forestlike patterns of the TWF graph; in the second phase, grant messages are echoed back from all active processes, simulating the granting of resources to requests. At the end of the second phase, all the processes that are not made active are deadlocked.

Because the system state is dynamic, the TWF graph may change during the execution of the algorithm. The algorithm overcomes such changes by propagating special Freeze messages throughout the system. When a process receives a Freeze message, it saves a snapshot of its state. Deadlocks are detected by running the deadlock detection algorithm on the collection of snapshots thus obtained.

## Hierarchical deadlock detection algorithms

In hierarchical algorithms sites are (logically) arranged in hierarchical fashion, and a site is responsible for detecting deadlocks involving only its children sites. To optimize performance, these algorithms take advantage of access patterns localized to a cluster of sites.

**Menasce-Muntz algorithm.** In the hierarchical deadlock detection algorithm of Menasce and Muntz,[3] all the resource controllers are arranged in tree fashion. The controllers at the bottommost level, called leaf controllers, manage resources; the others, called nonleaf controllers, are responsible for deadlock detection. A leaf controller maintains the part of the global TWF graph that is concerned with the allocation of the resources at that leaf controller. A nonleaf controller maintains the TWF graph spanning its children controllers and is responsible for detecting only deadlocks involving its own leaf controllers. Whenever a change occurs in a controller's TWF graph due to a resource allocation, wait, or release, the change is propagated to its parent controller. The parent controller makes the changes in its TWF graph, searches for cycles, and propagates the changes upward if necessary. A nonleaf controller can be kept up to date about the TWF graphs of its children continuously (that is, whenever a change occurs) or periodically.

**Ho-Ramamoorthy algorithm.** In the hierarchical algorithm of Ho and Ramamoorthy,[5] sites are grouped into several disjoint clusters. Periodically, a site is chosen as the central control site, which dynamically chooses a control site for each cluster (Figure 7). The central site requests every control site for its intercluster transaction status information and wait-for relations. As a result, a control site collects status tables from all the sites in its cluster and applies the one-phase deadlock detection algorithm to detect all deadlocks involving only intracluster transactions. Then it sends intercluster transaction status information and wait-for relations (derived from the information thus collected) to the central site. The central site splices the intercluster information thus received, constructs a system state graph, and searches it for cycles. Thus, a control site detects all deadlocks located in its cluster, and the central site detects all intercluster deadlocks.

## Future research directions

Several issues related to deadlock detection in distributed systems have not been adequately studied and require further research.

**Algorithm correctness.** There is a dearth of sophisticated formal methods to prove the correctness of deadlock detection algorithms for distributed systems.

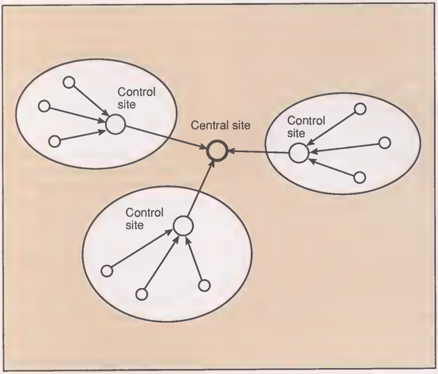

**Figure 7. Example of Ho-Ramamoorthy algorithm.**

Most researchers have used informal, intuitive arguments to show the correctness of their algorithms. But intuition has proved to be highly unreliable, and more than half the algorithms have been found incorrect. A formal proof of the correctness of deadlock detection algorithms is difficult for several reasons:

(1) The TWF graph and deadlock cycles can form in innumerable ways, making it difficult to imagine and exhaustively study all conceivable situations.

(2) Deadlock is very sensitive to the timing of requests.

(3) In distributed systems, message delays are unpredictable and there is no global memory.

Time-dependent proof techniques are particularly necessary.

**Algorithm performance.** Although many deadlock detection algorithms have been proposed for distributed systems, their performance analysis has not received sufficient attention. Most authors (for example, Obermarck and Sinha and Natarajan) have evaluated their algorithms on the basis of the number of messages exchanged to detect an existing cycle in the TWF graph. This performance criterion is deceptive because deadlock detection algorithms also exchange messages during normal conditions (when there is no deadlock). The number of messages exchanged may not be a true indicator of communication overhead because some algorithms[7,8,10] exchange long messages whereas others[1,3] exchange short messages. Therefore, we require a different criterion for computing communication overhead, which should take into account the number as well as the size of messages exchanged, not only in deadlocked conditions but also in normal conditions.

The persistence of deadlocks results in wasteful utilization of resources and increased response time to user requests. Therefore, an important performance measure of deadlock detection algorithms is the average deadlock persistence time. There is often a trade-off between message traffic and deadlock persistence time. For example, although the on-line deadlock detection algorithm of Isloor and Marsland detects a deadlock at the earliest instant, it has high message traffic. On the other hand, Obermarck's algorithm has less message traffic, but its deadlock persistence time is proportional to the size of the cycle. This trade-off is intuitive — quick detection of deadlock requires fast dissemination of information about the state graph, which implies high message traffic.

There is another dimension to the tradeoff between message traffic and deadlock persistence time. For example, Chandy, Misra, and Haas's algorithm requires short messages, but when it detects a deadlock, it takes a while to resolve it. In contrast, Haas and Mohan's algorithm exchanges longer messages; however, when a process detects a deadlock, it knows all the processes involved in it, and therefore the deadlock can be resolved quickly.

Besides communication overhead and deadlock persistence time, any evaluation of deadlock detection algorithms should consider measures such as storage overhead for deadlock detection information, processing overhead to search for cycles, and additional processing overhead to optimally resolve deadlocks. Among the factors that influence these measures are the techniques used for deadlock detection, the data access behavior of processes, the request-release pattern of processes, and resource holding time. How these factors influence performance and how the performance characteristics of different detection algorithms compare with each other are not well understood. A complete performance study of deadlock detection algorithms calls for the development of performance models, the measurement of performance using analytic or simulation techniques, and a performance comparison of existing algorithms.

**Deadlock resolution.** Persistence of a deadlock has two major disadvantages: First, all the resources held by deadlocked processes are not available to any other process. Second, the deadlock persistence time gets added to the response time of each process involved in the deadlock. Therefore, the problem of promptly and efficiently resolving a detected deadlock is as important as the problem of deadlock detection itself. Unfortunately, most deadlock detection algorithms for distributed systems do not address the problem of deadlock resolution.

A deadlock is resolved by aborting at least one process involved in the deadlock and granting the released resources to other processes involved in the deadlock. Efficient resolution of a deadlock requires knowledge of all the processes involved in the deadlock and all resources held by these processes. When a deadlock is detected, the speed of its resolution depends on how much information about it is available, which in turn depends on how much

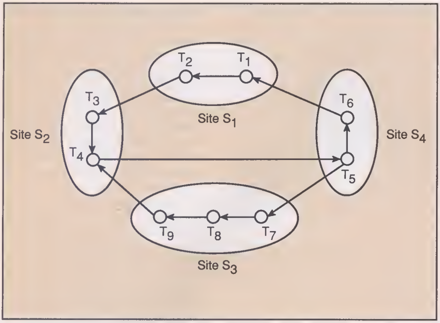

**Figure 8. Detection of a false deadlock.**

information is passed around during the deadlock detection phase. In existing distributed deadlock detection algorithms, deadlock resolution is complicated by at least one of the following problems:

- A process that detects a deadlock does not know all the processes (and resources held by them) involved in the deadlock — for example, the algorithms of Chandy, Misra, and Haas and Menasce and Muntz.
- Two or more processes may independently detect the same deadlock — for example, the Chandry-Misra-Haas and Goldman algorithms. If every process that detects a deadlock resolves it, then deadlock resolution will be inefficient because several processes will be aborted to resolve a deadlock (different processes may choose to abort different processes). Therefore, we need some postdetection processing to select a process to be responsible for resolving the deadlock.

Many deadlock detection algorithms require an additional round of message exchanges to select a deadlock resolver and/or to gather the information needed to efficiently resolve a deadlock. The Sinha-Natarajan algorithm is one of the exceptions where each deadlock is detected only by the highest-priority process that (upon deadlock detection) knows the lowest-priority processes in the deadlock cycle. There is often a trade-off between the volume of information exchanged during the deadlock detection phase and the amount of time needed to resolve a deadlock once it is detected. For example, Haas and Mohan's algorithm exchanges long messages, but when a deadlock is detected, its resolution is quick. On the other hand, in Menasce and Muntz's algorithm the messages exchanged are short, but when a deadlock is detected, its resolution is tedious and time consuming.

Whether it is better to exchange long messages during the deadlock detection phase and resolve a detected deadlock quickly or to exchange short messages during the deadlock detection phase and do extra computation to resolve a detected deadlock depends on how frequently deadlocks occur in a system. If deadlocks are frequent, then the former approach should perform better and vice versa. Even after all the information necessary to resolve a deadlock is available, resolution involves the following nontrivial steps:

(1) Select a victim (the process to be aborted) for the optimal resolution of a deadlock (this step may be computationally tedious).

(2) Abort the victim, release all the resources held by it, restore all the released resources to their previous states, and grant the released resources to deadlocked processes.

(3) Delete all the deadlock detection information concerning the victim at all sites.

Execution of the second step is complicated in environments where a process can simultaneously wait for multiple resources because the allocation of a released resource to another process can cause a deadlock. The third step is even more critical because if the information about the victim is not deleted quickly and properly, it may be counted in several other (false) cycles, causing detection of false deadlocks. As Choudhary et al. point out, the failure to delete probe messages in the Sinha-Natarajan algorithm causes the detection of false deadlocks. To be safe, during the execution of the second and third steps, the deadlock detection process (at least in potential deadlocks that include the victim) must be halted to avoid detection of false deadlocks. In the Sugihara et al. algorithm, a control token serializes global deadlock resolution to eliminate its side effects on the deadlock detection process.

*False deadlocks.* In environments where a process can simultaneously wait for multiple resources, deadlock resolution is even more complex because an edge may be shared by two or more cycles, and deleting that edge will break all those deadlocks. However, since the search for each cycle is carried out independently, deadlock detection initiated for some cycles may not be aware of the deleted edge, resulting in detection of false deadlocks. Figure 8 illustrates such a scenario. Two deadlocks share an edge ($T_4$, $T_5$). Suppose the top cycle has been detected by process $T_3$, which is breaking it by deleting the edge ($T_4$, $T_5$). Concurrently process $T_8$ may initiate a deadlock detection message, and it may happen that $T_3$ breaks the edge ($T_4$, $T_5$) after the deadlock detection message initiated by $T_8$ has crossed (or traversed) it. In this case, $T_8$ will detect a (false) deadlock involving processes $T_4$, $T_5$, $T_7$, $T_8$, and $T_9$, which has already been broken by $T_3$.

In brief, deadlock detection involves detecting a static condition — once a deadlock cycle is formed, it persists until it is detected and broken. On the other hand, deadlock resolution is a dynamic process — it changes the state graph by deleting its edges and nodes. Two forces are working in opposite directions: the wait for resources adds edges and nodes to the state graph, while deadlock resolution removes them from the state graph. Therefore, if deadlock resolution is not carefully incorporated into deadlock detection, false deadlocks are likely to be detected.

**Deadlock probability.** The frequency of deadlocks is a crucial factor in the design of distributed systems. If deadlocks are infrequent, then a time-out mechanism is the best approach to handling deadlocks because it has very low overhead. In a time-out mechanism a transaction or a process is aborted after it has waited for more than a specified period, called the time-out interval, after issuing a resource request. The most critical issue in a time-out mechanism is to choose an appropriate time-out interval; if the time-out interval is short, then many transactions may be aborted unnecessarily (that is, without being deadlocked), and if the time-out interval is long, then deadlocks will persist for a long time. The time-out mechanism is also susceptible to cyclic restarts, in which transactions are repeatedly aborted and restarted.

The probability of deadlocks depends on factors such as process mix, resource request and release patterns, resource holding time, and the average number of data objects held (locked) by processes. The probability of deadlocks is difficult to analyze because deadlock occurrence is highly sensitive to the timing and order in which resource requests are made. Gray et al.[16] have done an approximate analysis of deadlock probability and found that

(1) transaction waits and deadlocks are rare, but they both increase linearly with the degree of multiprogramming,
(2) most deadlocks are of length (size) two,
(3) deadlocks rise as the fourth power of transaction size, and
(4) waits rise as the second power of transaction size.

The probability of deadlock is an important parameter, and any further work in this direction will be a worthwhile contribution.

To sum up, of the three types of algorithms for detecting global deadlocks, distributed are the most prominent and most thoroughly investigated. All distributed deadlock detection algorithms have a common goal — to detect cycles that span several sites in a distributed manner — yet they differ in the ways they achieve this goal. The following are the most salient characteristics of these algorithms:

- *The form in which the algorithm maintains and passes around information about the process-resource interaction.* Goldman's algorithm uses *lists*, Hass-Mohan's and Obermarck's use *strings*, Isloor-Marsland's uses *sets*, and Menasce-Muntz's uses the *condensed TWF graph.*
- *The way the algorithm conducts the search for cycles.* Obermarck's algorithm sends lists of the edges of a directed path in the state graph; Chandy et al.'s and Sinha-Natarajan's circulate a probe message along the edges of the state graph; Menasce-Muntz's passes the condensed TWF graph; Mitchell-Merritt's passes a label.
- *The amount of information available about a deadlock when it is detected.* In the algorithms of Chandy et al., Menasce-Muntz, Sinha-Natarajan, and Sugihara et al., a process that detects a deadlock knows that it is deadlocked but does not know all the other processes involved in the deadlock; in Goldman's and Haas-Mohan's algorithms, a process that detects a deadlock knows all the other processes involved in that deadlock.

Although several deadlock detection algorithms have been proposed for distributed systems, a number of issues remain to be addressed. Future research should focus on efficient resolution of deadlocks, correctness of distributed deadlock detection, modeling and performance analysis of deadlock detection algorithms, and the probability of deadlocks in distributed systems. ☐

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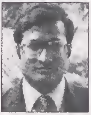

**Mukesh Singhal** is an assistant professor of computer and information science at Ohio State University, Columbus. His research and teaching interests are distributed systems, distributed database systems, and performance modeling of computer systems. From 1981 to 1985, he served as a research assistant and instructor in the Department of Computer Science, University of Maryland, College Park.

Singhal received a bachelor of engineering degree with distinction in electronics and communication engineering from the University of Roorkee, Roorkee, India, in 1980, and a PhD degree in computer science from the University of Maryland, College Park, in May 1986. He is a member of the Computer Society and the IEEE.

Singhal's address is Ohio State University, Dept. of Computer and Information Science, 2036 Neil Avenue Mall, Columbus, OH 43210.

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SPECIAL REPORT

# The 1987-88 Taulbee Survey Report

**David Gries and Dorothy Marsh**
**Cornell University**

**Mounting numbers and concern are both reflected in the Computing Research Board's report on the production and employment of PhDs and faculty in computer science and engineering.**

This report describes the results of a survey completed in December 1988 on the production and employment of PhDs and faculty in PhD-granting computer science/engineering departments during the 1987-88 academic year.* All 127 computer science (CS) departments (115 US and 12 Canadian) participated. In addition, 34 departments offering the PhD in computer engineering (CE) were included.**

Throughout this report, CE statistics are reported separately so comparisons with previous years can be made for CS. But the intent is to merge all statistics for CS and CE after several years.

Some highlights from the survey are:

- The 127 CS departments produced 577 PhDs, an increase of 24 percent over the previous year. Of the 577 PhDs, 309 were Americans, 30 Canadians, and 238 neither; 295 (51 percent) went into academia, 167 (29 percent) to industry, 20 (3 percent) to government, and 55 (10 percent) overseas; and one was self-employed and 11 were unemployed (28 were unknown).
- The 127 CS departments expect to produce 769 PhDs next year. This 33-percent expected increase is probably too optimistic, and we expect instead an increase of 21 percent, to 700.
- 1,113 students passed their PhD qualifying exams in CS departments, an increase of 10 percent over 1986-87.
- The 127 CS departments have 2,427 faculty members, an increase of almost 7 percent. Of the total, 939 were assistant professors, 659 were associate professors, and 829 were full professors.
- The 127 CS departments reported hiring 239 faculty and losing 177 (to retirement, death, other universities, graduate schools, and nonacademic positions).
- The 127 CS departments want to grow an average rate of 1.5 per department per year from 2,427 faculty members to 3,255 by academic year 1992-93 for an increase of 34 percent. (Last year, they wanted a growth of 1.7 per department but grew 1.2 per department.)

The growth of 24 percent in CS PhD production is almost twice what we expected. The growth in qualifying-exam passage in previous years and this year point to even more growth in PhD production, and we look forward to 650-700 PhDs in 1988-89. This is indeed satisfying, but at the same time a cause for concern. Continued steady growth for three to four more years could lead to overproduction. The field still expects to grow, and there won't be steady retirements to offset new PhD production for some 10 years.

The field continues to be far too young

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The title of this survey honors Orrin E. Taulbee of the University of Pittsburgh, who conducted these surveys for the Computer Science Board annually from 1970 to 1984. The Computer Science Board has since been renamed the Computing Research Board to incorporate computer engineering with computer science.

* Of the 157 departments completing the questionnaire, 148 departments reported on an academic-year basis and nine on a 1988 calendar-year basis.

** The Forsythe list, which contains all departments in the US and Canada that grant a PhD in CS or CE, is maintained by Terry Walker, a member of the Computing Research Board and its new executive director. This is the second year that the CE departments have been included.

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**Table 1. Titles of 157 departments.***

| Number | Title |
|---|---|
| 89 | Computer Science(s) |
| 22 | Electrical and Computer Engineering |
| 11 | Computer Science and Engineering |
| 10 | Computer and Information Science(s) |
| 7 | Electrical Engineering and Computer Science |
| 3 | Computer Engineering |
| 2 | Computing Science |
| 2 | Electrical Engineering |
| 2 | Information and Computer Science |
| 1 | Advanced Computer Studies |
| 1 | Applied Sciences |
| 1 | Computational Science |
| 1 | Computer Engineering and Science |
| 1 | Computer Science and Electrical Engineering |
| 1 | Computer Science and Operations Research |
| 1 | Electrical, Computer, and Biomedical Engineering |
| 1 | Mathematical and Computer Sciences |
| 1 | Mathematical Sciences |

* Instead of "department," the terms "center," "division," "program," and "school" were each used at least once.

and inexperienced, a problem that time alone is slowly solving. CS continues to have more assistant professors than full professors, which puts an added burden on the older people. In fact, the ratios of assistant and associate professors to full professors has not changed appreciably in four years. As we mentioned in previous Taulbee reports, no other field, as far as we know, has this problem. In fact, most scientific fields are 80 to 90 percent tenured in many universities. The CE departments have more full professors than assistant professors, mainly because many are older EE departments offering CE degrees. As will be discussed in the section entitled "PhD production and its growth," this problem is more severe at the newer and lower ranked departments; the top 25 departments have, for the second straight year, slightly more full professors than assistant professors.

The percentage of CS PhDs given to foreign students rose slightly from 40 percent to 41 percent. In CE, the percentage was much higher: 65 percent.

**Some methodological comments.** Questionnaires were sent to 127 CS PhD-granting departments and 34 CE PhD-granting departments in late October 1988. (The titles of the departments appear in Table 1).

All 127 CS departments and 30 of the 34 CE departments completed the questionnaire. Thus, the figures in this report are complete for CS. There was a marked improvement in the number of CE departments responding; we hope to have responses from all the CE departments in next year's survey.

The accuracy of this report depends, of course, on the accuracy of the individual departments in filling out the questionnaires. The new electrical engineering departments giving a PhD in CE had a more difficult time completing the questionnaire because they were asked to give information only on the CE part of their departments and the required information was difficult to extract.

As with most surveys, a small part of the data was not filled in or obviously was incorrectly entered. We took the liberty to adjust some figures and estimate a few others. For example, in a few cases, with 155 or 156 out of 157 departments reporting a figure in a field, we estimated that field for the others. Our goal was to make this report consistent, clear, and simple, without modifying the overall results in any way.

In some places, we analyzed the data for the higher ranked departments as compared to the lower ranked and unranked ones, using for ranking the 1980 survey done under the auspices of the National Research Council.[1] (We also included the two largest Canadian universities within the top 20.) The survey[1] is now nine years old, and many changes have occurred in CS since then (such as the emergence of more than 60 PhD-granting CS departments). Nevertheless, this breakdown still provides some useful comparisons.

To draw meaningful conclusions regarding growth of the field (using older surveys), we from time to time compare figures for the CS departments only, keeping figures for CE separate. We will combine CS with CE in several years. Throughout this report, figures for 1970-84 are taken from Taulbee,[2] for 1984-85 from Gries,[3] for 1985-86 from Gries,[4] and for 1986-87 from Gries and Marsh.[5] The figures for 1970-84 may not be accurate because not all departments completed questionnaires in those days.

## Data on students

**PhD production and its growth.** The field of CS produced 577 PhDs in 1987-88, an increase of 111 (24 percent) over 1986-87 and an increase of 347 (150 percent) over 1980. Table 2 shows the figures on PhD production for CS and CE, as well as for qualifying-exam passage and sizes of incoming classes.

**Table 2. PhD production and its growth.**

|  | Year | No. of Depts.* | PhDs Produced | Average Per Dept. | Qualifying Exam Passage | Average Per Dept. | New PhD Students | Average Per Dept. |
|---|---|---|---|---|---|---|---|---|
| CS | 1980-81 |  | 230 |  |  |  |  |  |
| CS | 1984-85 | 103 (109) | 326 | 3.2 | 755 | 8.2 | 1,177 | 12 |
| CS | 1985-86 | 117 (118) | 412 | 3.5 | 858 | 7.3 | 1,170 | 10 |
| CS | 1986-87 | 123 (123) | 466 | 3.8 | 1,008 | 8.2 | 1,430 | 12 |
| CS | 1987-88 | 127 (127) | 577 | 4.5 | 1,113 | 8.8 | 1,497 | 12 |
| CS-CE | 1986-87 | 145 (156) | 559 | 3.9 | 1,168 | 8.1 | 1,621 | 11 |
| CS-CE | 1987-88 | 157 (161) | 744 | 4.7 | 1,399 | 8.9 | 1,801 | 11 |

* The first number is the number of departments reporting, and the second number is the total of known PhD-granting departments.

**Table 3. PhD production in 1987-88 by ranking.**

| Rank | PhDs Produced | Average Per Dept. | PhDs Next Year | Average Per Dept. | Qualifying Exam Passage | Average Per Dept. | New PhD Students | Average Per Dept. |
|---|---|---|---|---|---|---|---|---|
| CS (all) | 577 | 4.5 | 769 | 6.1 | 1,113 | 8.8 | 1,497 | 11.8 |
| CS 1-12 | 162 | 13.5 | 200 | 16.7 | 248 | 20.7 | 360 | 30.0 |
| CS 13-24 | 87 | 7.3 | 118 | 9.8 | 175 | 14.6 | 238 | 19.8 |
| CS 25-36 | 69 | 5.8 | 114 | 9.5 | 166 | 13.8 | 165 | 13.8 |
| Other CS | 259 | 2.8 | 337 | 3.7 | 524 | 5.9 | 734 | 8.0 |
| CE | 167 | 5.6 | 206 | 6.9 | 286 | 9.5 | 304 | 10.1 |

**Table 4. Sex and minority status of the PhDs.**

|  | CS |  |  | CE |  |  | CS-CE |  |  |
|---|---|---|---|---|---|---|---|---|---|
| PhD Minority Status | Male | Female | Total | Male | Female | Total | Male | Female | Total |
| White, not of Hispanic origin | 340 | 49 | 389 | 56 | 4 | 60 | 396 | 53 | 449 |
| Black, not of Hispanic origin | 4 | 0 | 4 | 1 | 1 | 2 | 5 | 1 | 6 |
| Hispanic | 5 | 0 | 5 | 2 | 1 | 3 | 7 | 1 | 8 |
| Other | 168 | 11 | 179 | 101 | 1 | 102 | 269 | 12 | 281 |
| Total | 517 | 60 | 577 | 160 | 7 | 167 | 677 | 67 | 744 |

**Table 5. Sex, minority status, and citizenship of the CS PhDs since 1970.**

| Year | 70 | 71 | 72 | 73 | 74 | 75 | 76 | 77 | 78 | 79 | 80 | 81 | 82 | 83 | 84 | 84-85 | 85-86 | 86-87 | 87-88 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Total | 112 | 124 | 206 | 208 | 203 | 256 | 246 | 208 | 223 | 248 | 230 | 235 | 244 | 256 | 274 | 326 | 412 | 466 | 577 |
| Female | 1 | 4 | 12 | 7 | 6 | 21 | 14 | 14 | 19 | 24 | 28 | 26 | 27 | 31 | 29 | 32 | 50 | 51 | 60 |
| Percent | 1 | 3 | 6 | 3 | 3 | 8 | 6 | 7 | 9 | 10 | 12 | 11 | 11 | 12 | 10 | 10 | 12 | 11 | 10 |
| Black | 1 | 1 | 2 | 2 | 2 | 1 | 0 | 0 | 2 | 1 | 0 | 0 | 1 | 2 | 3 | 3 | 6 | 1 | 4 |
| Percent | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| Hispanic | No information |  |  |  |  | No information |  |  |  |  | No information |  |  |  |  | 7 | 6 | 8 | 5 |
| Percent |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 2 | 1 | 2 | 1 |
| Foreign | 22 | 21 | 39 | 41 | 46 | 68 | 57 | 68 | 51 | 65 | 82 | 79 | 83 | 86 | 87 | 122 | 184 | 181 | 238 |
| Percent | 20 | 17 | 19 | 20 | 23 | 27 | 23 | 33 | 23 | 26 | 36 | 33 | 34 | 34 | 32 | 37 | 45 | 40 | 41 |

As mentioned earlier, CS PhD-production increased 24 percent this year and 13 percent last year. Future growth is expected. Indeed, the 127 departments project 769 PhDs in 1988-89, a 33 percent increase. A more realistic estimate is 21 percent, to 700.

The projected future increases in PhD production are a matter of concern in the field. Estimates of the annual need for new PhDs range from 600 to more than 1,000, and the field is growing steadily to meet the need. However, growth in PhD production requires a commensurate growth in funding for research. Because of this interest in PhD production, we go into more detail on it in this report.

In 1987-88, an average of 4.7 CS-CE PhDs were produced per department (see Table 2), with 24 producing one, 18 producing two, 20 producing three, and 14 producing four (21 departments produced none). Thus, 97 departments produced less than the average and 60 departments more than the average. The 60 that produced more than the average — roughly 38 percent of the departments — produced 77 percent of the PhDs.

The over-average group of 60 expects to increase its PhD production in one year far less (by 86, or 15 percent) than the under-average group (by 145, or 82 percent). For both 1985-86 and 1984-85, the expected growth was about the same for the over-average group (24 percent), but is less (15 percent) for next year. Growth in the larger departments is slowing down. The predicted one-year growth by the under-average group was 167 percent in 1984-85, 164 percent in 1985-86, 116 percent in 1986-87, and 82 percent in 1987-88.

In an effort to find different expected-growth patterns, Table 3 presents the data for the groups of departments in various rankings.[1]

In 27 CS-CE departments, 15 or more students passed the qualifying examination. They accounted for 62 percent of the students passing the exam.

**Sex and minority status of the PhDs.** Table 4 gives the figures on PhDs awarded to minority students and females. The figures are rather depressing from the standpoint of minority and female representation in the field. Table 5 shows the statistics since 1970, with the data before 1984-

85 taken from Taulbee.[2] Throughout the 1980s, the percentages of PhDs who are women, black, and Hispanic have remained relatively constant at about 10 percent, 1 percent, and 2 percent, respectively.

**Table 6. Citizenship of the PhDs.**

| | US | Canadian | Foreign | Percent Foreign |
|---|---|---|---|---|
| CS | 309 | 30 | 238 | 41% |
| CE | 56 | 1 | 110 | 66% |
| CS-CE | 365 | 31 | 348 | 47% |

**Citizenship of the PhDs.** The number of PhDs given to foreigners increased from 181 to 238, although the percentage remained essentially the same as last year. Table 6 presents the citizenship figures of the PhDs. Table 5 contains the figures for foreigners from 1970 to 1988.

**Employment of the PhDs.** As Table 7 shows, 33 percent of the CS PhDs produced took positions outside academia in the US or Canada and 51 percent took faculty positions in the US or Canada. There was little change from the previous year, when the respective figures were 35 percent and 54 percent.

**Undergraduate and master's degrees.** Many universities and colleges have undergraduate and/or master's programs but do not award the PhD, so the data presented below says little about the field of computer science as a whole.

Table 8 gives statistics on undergraduate and master's degrees in PhD departments, with columns labeled "88-89" representing expectations. Although the average per department stayed about the same, the number of CS undergraduate degrees awarded increased by 219, partly because of the four new departments. The departments expect a 1-percent decrease next year.

**Table 7. Employment of the PhDs.**

| | | | | Academia | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Number of PhDs | Unemployed | Self-Employed | PhD Dept. | Not PhD Dept. | Not CS or CE | Industry | Government | Outside US and Canada | Unknown |
| CS | 577 | 11 | 1 | 229 | 58 | 8 | 167 | 20 | 55 | 28 |
| Percent | | 2% | 0% | | | 51% | 29% | 3% | 10% | 5% |
| CS-CE | 744 | 11 | 1 | 259 | 59 | 20 | 219 | 24 | 73 | 78 |
| Percent | | 1% | 0% | | | 45% | 29% | 3% | 10% | 10% |

**Table 8. Undergraduate and master's degrees.**

| Non-PhD Degrees, PhD Departments Only | | Undergraduate 84-85 | 85-86 | 86-87 | 87-88 | 88-89 | Master's 84-85 | 85-86 | 86-87 | 87-88 | 88-89 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CS | Number of degrees | 10,422 | 10,947 | 10,540 | 10,759 | 10,688 | 2,889 | 3,720 | 3,614 | 4,150 | 4,123 |
| | Number of depts. responding | 96 | 116 | 121 | 127 | 127 | 101 | 116 | 123 | 127 | 127 |
| | Average per dept. | 109 | 94 | 87 | 85 | 84 | 29 | 32 | 29 | 33 | 32 |
| CE | Number of degrees | | | 2,103 | 1,928 | 1,958 | | | 731 | 1,009 | 1,043 |
| | Number of depts. responding | | | 22 | 30 | 30 | | | 22 | 30 | 30 |
| | Average per dept. | | | 96 | 64 | 65 | | | 33 | 34 | 35 |
| CS-CE | Number of degrees | | | 12,643 | 12,687 | 12,646 | | | 4,345 | 5,159 | 5,166 |
| | Number of depts. responding | | | 143 | 157 | 157 | | | 145 | 157 | 157 |
| | Average per dept. | | | 88 | 81 | 81 | | | 30 | 33 | 33 |

**Table 9. New graduate students in fall 1988.**

| New Graduate Students | | Total New Graduate Students | With CS Degrees | PhD Program | Master's Only Program | Part-time Master's Students | Part-time Master's in Depts. With 6-50 |
|---|---|---|---|---|---|---|---|
| CS | Total | 4,067 | 1,901 | 1,497 | 2,503 | 1,107 | 708 |
| | Depts. responding | 127 | 118 | 127 | 127 | 125 | 47 |
| | Average per dept. | 32 | 16 | 12 | 20 | 9 | 15 |
| CE | Total | 1,054 | 162 | 304 | 750 | 562 | 200 |
| | Depts. responding | 29 | 27 | 29 | 29 | 28 | 11 |
| | Average per dept. | 36 | 6 | 10 | 26 | 20 | 18 |
| CS-CE | Total | 5,121 | 2,063 | 1,801 | 3,253 | 1,669 | 908 |
| | Depts. responding | 156 | 145 | 156 | 156 | 153 | 58 |
| | Average per dept. | 33 | 14 | 12 | 21 | 11 | 16 |

Table 10. New PhD students in CS departments.

| Departments | Number of Departments | Total | | | | Average | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 1985 | 1986 | 1987 | 1988 | 1985 | 1986 | 1987 | 1988 |
| Ranked 1-12 | 12 | 349 | 290 | 287 | 360 | 29 | 24 | 24 | 30 |
| Ranked 13-24 | 12 | 219 | 176 | 207 | 238 | 18 | 15 | 17 | 20 |
| Ranked 25-36 | 12 | 144 | 165 | 176 | 165 | 12 | 14 | 15 | 14 |
| All other | 62, 81, 85, 91 | 465 | 678 | 760 | 734 | 8 | 7 | 9 | 8 |

Table 11. Faculty statistics, 1988-89 academic year.

| Faculty Depts. | All CS-CE Depts. Total | All CS-CE Depts. Average | 127 CS Depts. Total | 127 CS Depts. Average | Top 25 CS Depts. Total | Top 25 CS Depts. Average | Other 102 CS Total | Other 102 CS Average |
|---|---|---|---|---|---|---|---|---|
| Tenure-track faculty | 2,990 | 19.0 | 2,427 | 19.1 | 699 | 28.0 | 1,728 | 16.9 |
| Assistant professor | 1,118 | 7.1 | 939 | 7.4 | 250 | 10.0 | 689 | 6.8 |
| Associate professor | 815 | 5.2 | 659 | 5.2 | 171 | 6.8 | 488 | 4.8 |
| Full professor | 1,057 | 6.8 | 829 | 6.5 | 278 | 11.1 | 551 | 5.4 |
| Non-teaching research faculty | 176 | 1.1 | 156 | 1.2 | 79 | 3.2 | 77 | 0.8 |
| Post-doctorates | 126 | 0.8 | 101 | 0.8 | 65 | 2.6 | 36 | 0.4 |
| Non-tenure-track teachers | 402 | 2.6 | 333 | 2.6 | 79 | 3.2 | 254 | 2.5 |
| Other faculty (e.g. visitors) | 258 | 1.6 | 228 | 1.8 | 85 | 3.4 | 143 | 1.4 |

Table 12. New PhD salaries for fall 1988.

| | All US CS-CE Depts. | All US CS Depts. | Top 24 US CS Depts. | Other 103 US CS Depts. | 12 Canadian CS Depts. |
|---|---|---|---|---|---|
| Total hired | 263 | 215 | 44 | 171 | 24 |
| Number of departments reporting salaries | 102 | 82 | 18 | 64 | 7 |
| Minimum | $38,000 | $38,000 | $40,000 | $38,000 | $34,322 |
| Average (of the averages) | $42,767 | $42,653 | $43,422 | $42,487 | $42,846 |
| Maximum | $48,000 | $47,000 | $47,000 | $45,600 | $47,300 |

**New graduate students in fall 1988.** Table 9 gives enrollment figures for new students in fall 1988. In the table, "PhD program" stands for the number of new graduate students in PhD programs, regardless of whether they intend to earn a master's degree first. The number of new graduate students in CS rose 12 percent from last year (from 3,644 to 4,067), and the number of new graduate students in CS PhD programs rose from 1,430 to 1,497.

The data for part-time master's students needs some explanation. Forty-five departments (or 5 percent) had no part-timers, and 30 departments had five or fewer part-timers. For these departments, the part-time master's program may be inconsequential — perhaps just a small employee degree program of the university. On the other hand, the two largest part-time master's programs had 149 and 100 new part-timers, respectively. The last column gives figures only for departments with between six and 50 new part-time master's students.

Table 10 gives the number of new PhD students in CS departments this year and the past three years, with departments grouped by rank.

## Faculty

Table 11 contains statistics on departmental faculty in September 1988. In the table, all numbers are in terms of "full-time equivalents." For example, two half-time appointments count as one position.

CS saw little change over last year in the proportions of faculty at the three levels. CS remained a relatively young field, with fewer full professors per department (6.5) than assistant professors (7.4). The top 25 departments have about the same number (11.1 and 10.0) of full professors and assistant professors per department.

**Hiring for 1988-89.** CS-CE departments reported hiring 264 new faculty — 1.7 per department. CS departments in the US hired 215 — 1.9 per department. Salaries were reported for new PhDs hired for fall 1988 by 102 US CS-CE departments, 82 US CS departments, and seven Canadian departments. Table 12 gives this salary information. The data for the Canadian universities are shown separately in Cana-

Table 13. New US PhD salaries for fall 1988 and three previous years.

| Salary (in thousands) | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1985-86: Number of depts. | 2 | 10 | 11 | 11 | 5 | 5 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1986-87: Number of depts. | 3 | 1 | 9 | 11 | 16 | 14 | 5 | 4 | 2 | 0 | 0 | 0 | 0 | 0 |
| 1987-88: Number of depts. | 1 | 1 | 1 | 3 | 8 | 13 | 14 | 20 | 4 | 1 | 1 | 0 | 1 | 1 |
| 1988-89: Number of depts. | 0 | 0 | 0 | 2 | 2 | 5 | 13 | 33 | 19 | 11 | 14 | 0 | 2 | 1 |

Table 14. Nine-month salaries, 113 out of 115 US CS departments.

| | | Reported Minimums | | | Average Over All | Reported Maximums | | |
|---|---|---|---|---|---|---|---|---|
| Faculty Rank | Number | Min. | Mean | Max. | Salaries | Min. | Mean | Max. |
| Assistant | 846 (854) | $30,000 | $40,932 | $47,800 | $43,959 | $35,312 | $46,479 | $59,600 |
| Associate | 564 (568) | 28,300 | 45,480 | 54,900 | 50,806 | 41,938 | 54,872 | 71,301 |
| Full | 705 (717) | 34,600 | 54,250 | 77,100 | 67,205 | 48,100 | 79,308 | 130,000 |

Table 15. Twelve-month salaries, 12 of 12 Canadian CS departments (Canadian dollars).

| | | Reported Minimums | | | Average Over All | Reported Maximums | | |
|---|---|---|---|---|---|---|---|---|
| Faculty Rank | Number | Min. | Mean | Max. | Salaries | Min. | Mean | Max. |
| Assistant | 85 (85) | $34,322 | $43,208 | $52,335 | $45,211 | $41,165 | $49,439 | $59,409 |
| Associate | 91 (91) | 39,800 | 50,673 | 60,000 | 58,381 | 53,176 | 66,326 | 103,000 |
| Full | 112 (112) | 53,520 | 61,708 | 67,245 | 72,616 | 71,591 | 84,568 | 106,074 |

Table 16. Salaries, 140 of 157 CS and CE US departments.

| | | Reported Minimums | | | Average Over All | Reported Maximums | | |
|---|---|---|---|---|---|---|---|---|
| Faculty Rank | Number | Min. | Mean | Max. | Salaries | Min. | Mean | Max. |
| Assistant | 1,016 (1,033) | $30,000 | $40,845 | $47,800 | $43,918 | $35,312 | $46,458 | $59,600 |
| Associate | 712 (724) | 28,300 | 45,306 | 54,900 | 50,261 | 41,000 | 54,256 | 71,301 |
| Full | 924 (945) | 34,600 | 53,673 | 77,100 | 66,318 | 45,000 | 78,355 | 130,000 |

dian dollars. Canadian salaries are on a 12-month scale, the Canadian and US dollars are different, and there are differences in the amount of consulting that typically can be performed by Canadian and US faculty members.

The average US salary for a new PhD increased from $36,668 in fall 1985 to $38,957 in fall 1986 (6.2 percent) to $40,885 in fall 1987 (4.9 percent) to $42,653 in fall 1988 (4.3 percent).

More information is included in Table 13, which gives the number of departments averaging a salary in each $1,000 range for fall 1988 and three previous years (numbers are rounded and presented in thousands of dollars).

The departments reported hiring faculty with PhDs earned in 1982 or later in a field other than computing science/engineering. The fields were electrical engineering (15), mathematics (4), applied mathematics (2), psychology (2), philosophy (1), physics (1), management sciences (1), applied linguistics (1), and industrial engineering (1). Part of the increase in the number of new faculty with electrical engineering degrees is due to the inclusion of the CE departments in the survey the past two years.

**Faculty salaries.** Table 14 summarizes nine-month faculty salaries in US departments, effective January 1989. Note that these salaries are given for the 1988-89 academic year, although other information contained in the report reflects the 1987-88 academic year. The second column in the table gives the number of faculty (in each rank) for which salaries were reported and,

Table 17. Desired faculty growth.

| | | 1988-89 | 1989-90 | 1990-91 | 1991-92 | 1992-93 | Four-Year Increase |
|---|---|---|---|---|---|---|---|
| CS | Faculty size | 2,427 | 2,684 | 2,860 | 2,998 | 3,255 | 34% |
| | Average size | 19.1 | 21.1 | 22.5 | 23.6 | 25.6 | |
| CS-CE | Faculty size | 3,094 | 3,339 | 3,544 | 3,703 | 3,980 | 29% |
| | Average size | 19.8 | 21.4 | 22.7 | 23.7 | 25.5 | |

Table 18. Average desired four-year growth in CS departments.

| | By Rank | | | | By Department Size | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Per department | 1-12 | 12-24 | 24-36 | rest | 1-9 | 10-19 | 20-29 | 30-39 | 40-49 |
| Number of depts. 1988-89 | 12 | 12 | 12 | 91 | 8 | 67 | 34 | 12 | 5 |
| Average dept. size 1987-88 | 30 | 26 | 21 | 16 | 7 | 14 | 24 | 34 | 43 |
| Average dept. size 1988-89 | 31 | 26 | 23 | 17 | 8 | 15 | 24 | 33 | 43 |
| Average dept. size 1992-93 | 35 | 31 | 30 | 23 | 12 | 22 | 30 | 36 | 50 |
| Average four-year increase | 4 | 5 | 7 | 6 | 4 | 7 | 6 | 3 | 7 |
| Percent growth (projected) | 13% | 19% | 30% | 35% | 50% | 47% | 25% | 9% | 16% |

Table 19. Faculty losses.

| | CS-CE Depts. | | | CS Depts. | | |
|---|---|---|---|---|---|---|
| | With PhD | Without PhD | Total | With PhD | Without PhD | Total |
| Died or retired | 18 | 6 | 24 | 13 | 4 | 17 |
| Were visitors, returned to employer | 22 | 3 | 25 | 22 | 3 | 25 |
| Teaching elsewhere | 70 | 2 | 72 | 60 | 2 | 62 |
| Left for nonacademic positions | 48 | 3 | 51 | 45 | 3 | 48 |
| Returned to graduate school | 0 | 6 | 6 | 0 | 6 | 6 |
| Other | 16 | 6 | 22 | 13 | 6 | 19 |
| Total | 174 | 26 | 200 | 153 | 24 | 177 |

in parentheses, the total number of faculty in that rank.

Departments reported the minimum, mean, and maximum salaries of assistant, associate, and full professors and the number of faculty in each rank. For minimum salaries (and for maximum salaries), the table shows the minimum, average, and maximum. Finally, the average is given over all salaries in each faculty rank; this is not the average of the means, but the true average.

Comparing this year's CS figures with last year's, we find that the average assistant professor salary rose 4.8 percent from $41,945 to $43,959, the average associate professor salary rose 7.1 percent from $47,428 to $50,806, and the average full professor salary rose 6.6 percent from $63,037 to $67,205.

Thirty-five US departments reported a maximum full-professor salary of greater than $90,000.

Table 15 gives salary information for the 12 Canadian departments. Table 16 gives the information for all US CS and CE departments.

**Estimates of department growth by 1992-93.** The departments were asked to estimate their faculty sizes through 1992-93 (see Table 17), given an adequate supply of applicants (the lack of applicants has been a problem in the past). The 157 CS-CE departments would like to grow by 886 (29 percent) by 1992-93. The 127 CS departments would like to grow by 778 to a total of 3,255 (25.6 faculty per department). Last year, the 123 departments expected to grow to 3,133 (25.5 per department) by 1992-93, so the expected growth has not changed appreciably.

Last year, the 123 departments reported a desire to grow from 2,325 (18.9 per department) in 1987-88 to 2,543 (20.7 per department) faculty members by 1988-89. However, 127 CS departments this year reported growing only to 2,427 (19.1 per department). Table 18 indicates that all departments desire substantial growth, but with the most growth expected in the lower-ranked and smaller departments.

**Faculty losses.** Table 19 gives statistics on faculty losses. The CS departments reported losing 0.7 percent of the faculty through death and retirement, and the CE departments reported losing 1.1 percent. We don't expect higher percentages of retirement in CS for another 5-10 years. Of the other 200 CS-CE faculty who left, at least 35 percent assumed other teaching positions, 26 percent exited academia, 13 percent were visitors who returned to their employers, and 3 percent returned to graduate school. The percentages for CS were very similar: 35 percent teaching elsewhere, 27 percent filling positions outside academia, 14 percent being visitors, and 3 percent returning to graduate school. This year, 177 faculty left the departments; last year, 179. ☐

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**David Gries** has been at Cornell University since 1969 and served as Computer Science Department chair from 1982 to 1987. He received his doctorate from the Munich Institute of Technology in 1966. Gries was a co-recipient of the ACM Programming Languages and Systems Best Paper Award in 1976, was a Guggenheim Fellow in 1984-85, and received the AFIPS Education Award in 1985.

**Dorothy Marsh** has been employed at Cornell University since 1984 and has been an administrative assistant in the university's Computer Science Department since 1986. She previously worked with the US Department of Agriculture. Marsh is also a part-time student at Cornell.

The authors' address is Computer Science Department, Upson Hall, Cornell University, Ithaca, NY 14853-7501.

For a complete copy of this year's Taulbee Survey, including five additional tables, see pp. 1,217-1,224 of the October 1989 issue of *Communications of the ACM*.

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Two reports from the IEEE Scientific Supercomputer Subcommittee: The first report traces and analyzes the evolution of computer classes and offers near-term projections; the second updates a 1983 report on supercomputer hardware.

# The Computer Spectrum

## A Perspective on the Evolution of Computing

Since the mid-1950s, the modern computer has been evolving to satisfy the diverse computational needs of an increasingly large part of society. Various classes of computers have emerged, until the computers in widespread use today span a range of sizes and applications greater than that of any other manufactured product.

The cost of manufactured items that might properly be called computers ranges from $20 for hand-held programmable devices to more than $20 million for the largest supercomputer systems in the marketplace today — a factor exceeding $10^6$ in cost and a similar factor in terms of computational power and storage capacity. Although their range is not quantifiable, the breadth of applications for which these computers are used is equally impressive.

To satisfy this broad spectrum of use and to accommodate the pocketbooks of potential customers, computer manufacturers continue developing — at a dizzying rate — new types of computers and specialized software for particular market niches. In fact, the options available are an elegant example of the diversity that mass production has produced in the modern world, as so pointedly observed by Alvin

### Participating members of the IEEE Scientific Supercomputer Subcommittee

The IEEE Scientific Supercomputer Subcommittee is a technology-policy committee under the IEEE United States Activities Board, 1828 L St., NW, 12th Floor, Washington, DC 20036.

The committee members participating in the development of these reports are Alfred E. Brenner, Supercomputing Research Center, Bowie, Md.; Sidney Fernbach (chair), consultant, San Jose, Calif.; Duncan Lawrie, Center for Supercomputing R&D, University of Illinois, Urbana; Alan McAdams, Cornell University, Ithaca, N.Y.; Kenneth W. Neves, Boeing Computer Services, Seattle, Wash.; John M. Richardson, National Research Council, Washington, DC; John P. Riganati, Supercomputing Research Center, Bowie, Md.; Stewart Saphier, Department of Defense, Washington, DC; Paul B. Schneck, Supercomputing Research Center, Bowie, Md.; Lloyd Thorndyke, St. Paul, Minn.; and Hugh Walsh, IBM Data Systems Division, Kingston, N.Y.

Additional committee members contributing to the supercomputer hardware report include Lara Baker, consultant, Los Alamos, N.M.; Vito Bongiorno, Cray Research, Mendota Heights, Minn.; James F. Decker, Dept. of Energy, Washington, DC; Dieter Fuss, Lawrence Livermore National Laboratory, Livermore, Calif.; and Norman Morse, Los Alamos National Laboratory, Los Alamos, N.M.

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Toffler in *Future Shock*.[1]

Although a multitude of terms in use today identifies classes of computers, there seems to be little precision or agreement on these classifications. This report classifies computer systems and reviews their evolution. Then, with the hindsight of this historical analysis, it provides near-term projections of further changes and evolution.

## The first two classes: business and scientific computers

In the early days of the modern computer era, that is, during the 1950s, all machines were thought to be equally useful on all problems. The range of applications was quite diverse, but the extent of use quite limited. The computers used either binary or decimal numerical representations.

Soon, two marketplaces developed: one for business applications and the other for scientific applications. For business applications, fixed-point decimal arithmetic seemed in order; for scientific applications, floating-point binary arithmetic seemed preferable. These differences persist generally until the present day.

During the late 1950s and early 1960s, the two marketplaces developed more or less as separate entities with separate cultures. Typically, computer architectures focused on one or the other marketplace. However, starting with IBM's 1964 announcement of the System/360,[2] manufacturers attempted to coalesce at least the hardware satisfying both marketplaces.[3-5] Thus, the architecture of medium- to large-scale computers developed in the mid-1960s included both decimal and floating-point arithmetic. Unified operating systems were also introduced, but separate high-level languages and applications packages were developed to meet each market's specific needs. Through the 1970s and 1980s, these machines evolved into general-purpose computing engines capable of serving both classes of use. Today, they are called mainframes.

## The emergence of new classes: the supercomputer and the minicomputer

A persistent, major demand for scientific computers more powerful than existing mainframes began in the 1960s. Driven by the US government's national security needs and by the meteorological and seismic communities' needs, a new market niche developed at the very high end of the scientific computing spectrum. The computers serving this market, the most powerful scientific computational systems available, have come to be called supercomputers.*

The demand for faster computer performance for scientific problems has persisted for almost four decades. In about the mid-1970s, supercomputer capability crossed a critical threshold that allowed for the explosive development of "computational science," which now stands, de facto, alongside the theoretical and experimental sciences as a fully legitimate field. In almost every scientific and engineering discipline, technology development is relying more and more heavily on computer simulation, since only a small fraction of desirable experiments can be physically carried out cost-effectively or realistically. This reliance on simulation has fueled the ever-increasing demand for scientific computing power.

Early in the modern computer era, the technical and business communities rose to the challenge of putting computers to active use. However, all early systems were both large and costly. High cost inhibited the proliferation of mainframe systems, yet a large market awaited computers with substantially lower price tags. A new class of computer system — the forerunner of today's minicomputer — with lower computational speed but more than proportionally reduced cost was introduced, primarily by new companies. Early examples were Digital Equipment Corporation's PDP 1 and IBM's 650.[6,7] Other entries from additional manufacturers soon followed. Thus, by the mid-1960s, although the general scientific and business marketplaces were still distinct, three types of products were available: minicomputers, mainframes, and supercomputers.

As with all new products, variations soon appeared to meet the requirements of different market niches. The major categories remained, but new systems were introduced with variations in performance, size and kind of memory, word length, and types of instructions. Software was further diversified to address the particular needs of the wide variety of users. Price, size, ease of use, and relative performance remained the major factors determining the success of the various offerings, with price the most important single factor, then as now. For example, minicomputers established a price niche, but price and performance still vary widely, from quite small minicomputers to high-end superminicomputers that are larger and more capable than many low-end mainframes.

## The evolution of the supercomputer

The 1970s saw the first appearance of two architectural features — vector processing and parallel processing — that would have widespread repercussions.[8] These features were typified by the Star 100, a vector machine built by Control Data Corporation, and the Illiac IV, a parallel processor designed at the University of Illinois and built by Burroughs Corporation.[9-14] Of the two approaches, vector processing was introduced first into commercial supercomputers and gave rise to major performance improvements. However, additional gains through architectural, technological, and software improvements to this approach are reaching saturation. The technology used by successive generations of supercomputers is slowly reaching natural limits imposed by the speed of light and by the materials used for the processes on which the technological improvements are based. Consequently, major performance gains must now come from architectural designs capable of parallel processing on a single computation. All high-performance computer vendors are introducing this approach into their product lines.

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*A definition of supercomputer(s) as given in "Supercomputing, An Informal Glossary of Terms," prepared by the Scientific Supercomputer Subcommittee of the IEEE Committee on Communications and Information Policy: "At any given time, that class of general-purpose computers that are both faster than their commercial competitors and have sufficient central memory to store the problem sets for which they are designed. Computer memory, throughput, computational rates, and other related computer capabilities contribute to performance. Consequently, a quantitative measure of computer power in large-scale scientific processing does not exist and a precise definition of supercomputers is difficult to formulate."

Over the years, technological advances have enabled increased supercomputer performance at essentially constant total system prices. Typically, supercomputer acquisition costs range from $10 million to $20 million. Despite the rapidly falling price/performance ratio, the high cost of acquisition inhibits widespread use of supercomputers, even in cases where the life-cycle payoff far exceeds the investment.

To make supercomputers more readily available to a broader group of users, high-performance wide-area networks are being introduced. These networks allow effective remote access to costly supercomputer facilities. Communication lines, operating at the highest commercially available speed, interconnect user equipment at local sites to remote supercomputers. Often, to avoid burdening the supercomputer with communications overhead, front-end computers or other smaller computer systems at the supercomputer site handle communications. The capabilities of the front-end computers vary widely according to what is readily available or affordable to the given user.

Because of the high cost of supercomputers and the additional complications of accessing such facilities remotely, there are strong pressures to find alternative solutions. Thus, the search continues for more readily available, less expensive, computing resources. When smaller mainframes or even minicomputers are adequate to solve a user's problem, such alternatives work well, but only because the problem does not require a supercomputer. Many problems have such demanding computing requirements that only facilities with supercomputer performance levels are appropriate.

## The emergence of the minisupercomputer

By the 1980s, these pressures led to yet another category of computer, the minisupercomputer. These relatively inexpensive, readily available, high-performance computing engines are architecturally similar to supercomputers, but are typically built using the assembly-line manufacturing methods of minicomputer vendors. Their lower cost makes them available to small groups of users, for example, departments within a company or university. As in the past, new players saw this market niche developing and are trying to fill the gap.

The minisupercomputer's design favors economy — not performance — in contrast to the performance-over-cost tradeoff driving supercomputer design. In many senses, it has given rise to what might be called the "personal" supercomputer, and demand for such economical machines is high in industry and the research community. It's too early to determine breadth of funding, but this class of system appears to be the budget-conscious scientist's and engineer's preferred alternative to remote access to a supercomputer. With these systems, the user has the advantage of local control of the resource.

Two technological elements, the microprocessor and parallel processing, are having a major impact on the development of minisupercomputers. The microprocessor — a full-fledged processor on a chip — made possible the development of the low-cost personal computer, whose sales now number in the millions of units. Revenue from personal computers, in turn, fueled the development of even more powerful microprocessors. Incorporating these microprocessors into parallel processing architectures let many universities and small firms engage in low-cost experimentation with parallel processing. This has given rise to many quite modest, mostly start-up commercial entities that compete for the broadening minisupercomputer market.

The minisupercomputer will not supplant the supercomputer. There will always be a need for larger and faster machines. However, there will also be a need for less costly systems (minisupercomputers) to serve as stand-alone systems, distributed departmental-level systems, and powerful front ends.

## Other important classes: the personal computer and the applications workstation

Apple Computer introduced its inexpensive, "user-friendly" personal computer in 1977.[15] Although not the first personal computer, the product rapidly established a new niche in the marketplace, primarily because of its low cost and powerful processing capability. More importantly, the new system required very little user training. IBM, recognizing a new mass-market potential, entered this low-cost product arena in 1981. These two firms are now the major players in this market, a niche quite removed from previous classes of computers.

Personal computers started as expensive toys; electronic games were a major use in their early days. With time, more serious activities, especially word processing, spreadsheets, and database systems, became their primary function. These machines have transformed the office into today's "electronic office." The breadth of their application has increased enormously, and their performance and price now span a wide range.

More recently, specialized, very powerful classes of personal computers have entered the marketplace. Initially called scientific workstations, they have evolved into more-general applications workstations. Their computing performance and price levels range from the high end of the personal computer niche into the former province of the minicomputer and low-end mainframe. This class of desktop system was driven by the rapid evolution of microprocessors into powerful single-chip processors mass-produced at remarkably low cost. Only a few years ago, systems of similar power required investments in excess of $100,000 and took up a good fraction of an air-conditioned room. Now, applications workstations have blossomed into a major industry with a well-established market niche. Their low cost, high performance, personalization, and dedication to an individual's needs make them very attractive products.

## Historical analysis

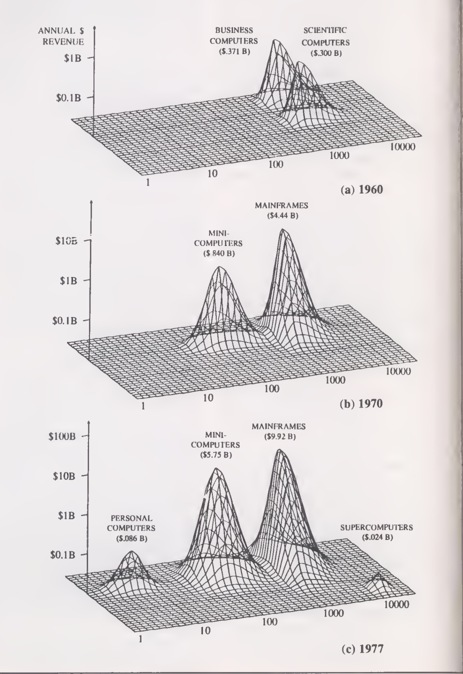
The evolution of the computer industry can be traced according to (1) applications served, (2) individual system cost, and (3) total annual revenue in each market segment. In the figure at right, five representative snapshots of computer industry development show the market niches appropriate to each year. The "applications" axis is a qualitative one, divided into "scientific" and "business" applications. The "unit cost" axis shows the price of the various systems, stated in thousands of dollars of the given year. The vertical axis shows "annual dollar revenue" for each market segment, again stated in dollars of the particular year.* The latter two axes use logarithmic scales to accommodate the range.

In 1960 (graph (a)), computer revenue was almost $700 million. At that time, there was a well-defined bifurcation of scientific and data-processing (business) computing, each served by different computer models.

Between 1965 and 1975, the minicomputer market emerged and took on a substantial fraction of the workload. During that period, as shown in the graph for 1970 (b), the emergence of the general-purpose mainframe coalesced the scientific and commercial marketplaces.

From 1975 to 1980, with 1977 shown as a representative year (c), the supercomputer market emerged in response to a need at the high end of scientific computing applications. This graph also shows the beginning of the personal computer market, quite separate in its early days from the other "serious" computing systems.

During the first half of the 1980s, growth continued in all market segments; the fourth graph (d) depicts the situation for 1982. The scientific workstation emerged, spanning the space between the personal computer and the minicomputer.



(a) 1960

(b) 1970

(c) 1977

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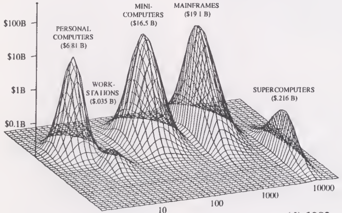
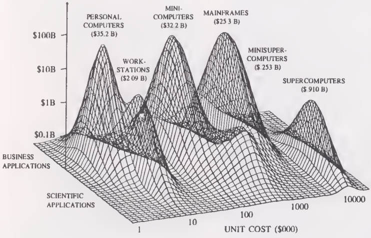
*Although "unit cost" and "annual dollar revenue" may be described in quantitative terms, these numbers are difficult to obtain with precision. There are questions such as whether or not the cost of peripherals and software is included. Indeed, is a disk — necessary for a system to function — included as part of the system or as a separate peripheral? Also, the demarcations between some of the categories, for example, minicomputers and mainframes, are likely to be made differently by different manufacturers. Thus, the more quantitative axes also must be interpreted as having quite large uncertainties.

The most current profile (e) uses preliminary 1987 data. It shows continued growth in all market segments and the initial development of the latest niche — the minisupercomputer.

At every step, other classes of computers were developed but failed to achieve significance as identifiable market segments. Some of them — for example, attached array processors — are still marketed. Because their dollar volume has remained limited, however, they do not appear in the graphs. In many cases, the uses of array processors have gradually been satisfied by other products.



**(d) 1982**



**(e) 1987**

**The changing profile of computing space over the last three decades: (a) 1960; (b) 1970; (c) 1977; (d) 1982; (e) 1987. The annual revenue peak represents total sales worldwide in dollars current for the year listed. Note that logarithmic scales are used for the unit cost and annual revenue axes.**

Sources: primary data, Dataquest; additional and corroborating data, Hambrecht and Quist and the Gartner Group.

The current annual revenue of the US computing industry exceeds $100 billion. The industry continues to be one of the fastest growing components of the US economy. Given the especially strong entrepreneurial spirit in the electronics and computer components of our industrial society, there continue to be new attempts to develop heretofore unrecognized niches. Many of these efforts fail because the ideas are unsound or poorly implemented or, as frequently happens, the timing is not right. Nevertheless, we can expect continued evolution and new niches in the marketplace.

## The missing element in the analysis: software

Effective use of any hardware system requires appropriate software. However, software's level of maturity is well behind that of hardware, to some extent because of the lower level of maturity of our software experience. The manufacture of electronic hardware items in our industrial base goes back more than half a century. In light of this experience, our schools address hardware in a mature engineering and production sense. This is not the case with software.

One problem is that software not only is much newer in concept, but also has far more implementation options than hardware. In contrast to the situation 20 or more years ago when early computer systems were delivered, the software efforts required to build a system today are much more demanding than the hardware development efforts. Most firms have not adequately integrated this new relationship into their planning and development cycles.

Sensible software developments are further hampered by the fact that there are few well-accepted standards to which designers must conform. The user sees the software more than the hardware when interacting with computer systems. So, to differentiate their products, many manufacturers have resisted agreeing to proposed industry-wide standards. Some have explicitly extended their software beyond the standard even when one exists. These are serious problems hampering the growth of the computing industry.

Until software reaches the maturity level of hardware, computing investments will not produce optimal returns. This is especially true of supercomputer software, since these systems play such an important role in advancing US technology. A solution to this problem is imperative, but it is often hindered by industry's short-term need for profitability. Thus, to ensure a solution, the government needs to actively foster research, development, and industrial coordination (for specific recommendations, see the committee's 1988 supercomputer software report[16]).

## The future spectrum

How will the computer industry evolve during the next decade?

One developing area is universally available networking. Computer networks are becoming important in every facet of research and industry. The merging of the communications and computing industries continues slowly and erratically, but inexorably. The growth of very high bandwidth communications links across the country is driven by customers' needs to transmit large quantities of data. Included are customers with science, research, commercial, and consumer-based needs (the latter arising especially from the entertainment industry). The collective demands of these users will ensure the development of basic, affordable, universally available networking.

At present, networking concepts are immature. Although conceptual standards have been adopted, the situation remains chaotic. Networking is passing through a "Tower of Babel" period where communications between different entities invariably have major complications. Manufacturers usually solve problems with their own product lines quickly and well, but communication between units of disparate manufacture generally remains an unsolved problem. The century may end before networked computer communication approaches the universality of today's telephone system.

As communication problems are solved, we expect some market niches to coalesce. Certainly there will continue to be very powerful computing engines, the supercomputers, for solving the most demanding computational problems. Also, there will be mainframes appropriate to massive data processing and management of large files, whether centralized or distributed. The largest of each of these systems will certainly rely on parallel processing to attain required performance levels. They may or may not use vector processing as well. The appearance of the architecture will depend on the successful conclusion of current research and product development programs. The level of parallelism — from a modest few or few-hundred processors up to a count in the thousands — is an open question. Much progress must be made, especially in software, before that question can be answered. We expect, however, that a wide range of parallelism will be explored for a long time.

Because of their lower cost, minisupercomputers and minicomputers are likely to continue as identifiable sub-markets. However, the demarcation between the minicomputer and the applications workstation and possibly between the minicomputer and the larger mainframes may disappear.

Good networking and good inter-unit communications will provide a wide breadth of options. Which options are used will be determined by the cost, the nature of the problem, the size and type of databases accessed, organizational division lines, and the local computer cultural precedents.

For almost all users, but especially for the scientific and engineering communities, desktop graphics (including color) will certainly play a major role. Also, the user-friendly tools that have become the norm for the personal computer will continue to be extended to span almost all human/computer interfaces.

Applications software will continue to evolve explosively. The user will become further and further relieved of understanding the working innards of the computer. Which computer in a network is being used will become of less interest to the user and, possibly, knowable only on explicit demand. Higher level languages will continue to evolve to accomplish these objectives.

What a user in any discipline wants is an unobtrusive desktop device through which requests can be made and responses received in as short a time as possible. Ideally, the workstation or device will be inexpensive, generate little noise and heat, take up little space on the desk, yield output as required, and make hard copy unobtrusively and quickly. Whether the actual processing components are in the box, down the hall, or in a central location some distance away (possibly across the country) should be of no consequence to the user.

What will the computer spectrum of 1995 or 2000 look like? It is safe to predict that the trends of the last 30 years will continue; niches will continue to evolve and revolutions in thought will continue to be ameliorated by the pragmatic realities of the marketplace. Over two millennia ago, Heraclitus stated, "Nothing endures but change." In our day, as Toffler warned, dramatic change has itself become a stable process.[1] Nowhere is this more evident — and more satisfying — than in the computer spectrum.

## Acknowledgments

We would like to acknowledge the assistance of Neil Coletti of the Supercomputing Research Center staff for the graphical presentation. We also thank Heidi James, the former IEEE staff member responsible for innumerable activities that made this report possible.

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# Supercomputer Hardware

## An Update of the 1983 Report's Summary and Tables

In 1983, the IEEE Scientific Supercomputer Subcommittee issued a report on supercomputer development in the US and abroad and recommended some government actions to support US leadership. The subcommitte recently reviewed its 1983 findings, taking into consideration the following changes in the supercomputer industry:

(1) Control Data Corporation spun off, subsequently reabsorbed, and on April 17, 1989, eliminated its supercomputer manufacturing facility, ETA Systems.

(2) A group of former Cray Research employees left Cray to start a new company, Supercomputer Systems, subsequently supported by IBM.

(3) On May 15, 1989, Cray Research split off a separate entity, the Cray Computer Corp., to manufacture the Cray-3 computer.

(4) IBM reentered the supercomputer business by the attachment of a vector facility to the 3090S mainframe. This system is in the low- to middle-performance range of supercomputer systems and had total sales at the end of 1988 of approximately 300 systems.

(5) NEC announced on April 10, 1989, its new high-performance line of computers including multiprocessor models. This is the first announced Japanese product with more than a single processor.

With these developments as background, the subcommittee reconsidered the topic and is reiterating the 1983 report's recommendations. (Recent reports of the Office of Science and Technology Policy/Federal Coordinating Committee for Science, Engineering, and Technology (OSTP/FCCSET) urge similar actions.) The subcommittee found that the 1983 report remains both a valid and current description of actions the US must undertake in the supercomputer hardware area.* In 1983, the hope for these actions was to maintain our lead. In 1989, this hope remains, but we are very close to having to regain rather than maintain our lead.

In summary, the subcommittee's recommendations in 1983 and again in 1989 are that the federal government

(1) Make a commitment to maintain leadership in scientific supercomputer development with a well-defined, long-range national program.

(2) Encourage both the continued development of scientific supercomputers and their availability to industry through the research community by adopting such measures as

- direct support for development of new supercomputer generations,

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*The subcommittee has reissued the 1983 document with an addendum, reprinted here, containing updated tables and figures on supercomputing. For a copy of the complete report, contact Deborah Rudolph, Technology Activities Council, IEEE-USA Washington Office, 1828 L St., NW, 12th Floor, Washington, DC 20036.

**Table 1. Current vector-architecture supercomputers by manufacturer and series, using data for the largest member of the series (all use 64-bit words).**

| | Cray X-MP | Cray-2 | Cray Y-MP |
|---|---|---|---|
| Announcement of series | — | — | Feb. 1988 |
| First installation of series | June 1983 | Oct. 1984 | Oct. 1988 |
| Number of processors | 1,2,4 | 1,2,4 | 1,2,4,8 |
| Peak performance | | | |
| Per processor | 235 Mflops | 488 Mflops | 333 Mflops |
| Total peak performance | 940 Mflops | 1,951 Mflops | 2,670 Mflops |
| Cycle time | 8.5 ns | 4.1 ns | 6 ns |
| Maximum main memory* | 0.5 Gbyte | 4 Gbyte | 1 Gbyte |
| Extended memory | 4 Gbyte | — | 4 Gbyte |
| Technology | | | |
| Logic | 16 gate ECL | 16 gate ECL | 2,500 gate ECL |
| (gate delay) | (650 ps) | (650 ps) | (350 ps) |
| Main memory | 64K CMOS | MOS 1M DRAM | ECL |
| (cycle time) | (68 ns) | (185 ns) | (30 ns) |
| | 64K ECL SRAM | 256K SRAM | |
| | (34 ns) | (54 ns) | |
| I/O storage: disk; solid-state secondary | | | |
| No. paths (total) | 32;2 | 36;— | 48;4 |
| Max. data rate path | 26.6;1,250 Mbytes/s | 26.6,500;— Mbytes/s | 26.6;1,250 Mbytes/s |
| Max. aggregate data rate | 400;2,500 Mbytes/s | 2,000;— Mbytes/s | 800;5,000 Mbytes/s |
| Cooling | Freon | Liquid immersion<br>(Fluorinert) | Fluorinert (CPU, memory)<br>Freon (I/O) |
| Operating systems | CTSS/COS/Unicos | Unicos/CTSS | CTSS/COS/Unicos |
| Languages/compilers | Fortran 77, C<br>Pascal, Ada | Fortran 77, C<br>Pascal, Ada | Fortran 77, C,<br>Pascal, Ada |
| Features | | | |
| Pipes (vector) | 4 Add | 4 Multiply | 8 Add |
| | 4 Logical | 4 Add | 8 Logical |
| | 4 Shift | 4 Logical | 8 Shift |
| | 4 Popcount | 4 Integer | 8 Popcount |
| | 4 FP Multiply | 4 Popcount | 8 FP Multiply |
| | 4 FP Add | | 8 FP Add |
| Load/store | 8 Loads<br>and 4 Stores | 4 Loads<br>or 4 Stores | 16 Loads<br>and 8 Stores |
| Registers, words per processor | | | |
| Scalar | 64B,64T,8A,8S | 8A,8S | 64B,64T,8A,8S |
| Vector | 512 = 8×64 | 512 = 8×64 | 512 = 8×64 |
| Other | | No chaining; local memory<br>(128Kbyte/processor) | |

*In units of $2^{30}$ bytes = 1,073,741,824, often called a gigabyte (even though it is 7 percent larger)

| CDC/ETA 10G | IBM 3090S | Fujitsu/Amdahl VP400E | Hitachi S-820-80 | NEC SX 2 |
|---|---|---|---|---|
| Oct. 1985 | — | Apr. 1982 | Aug. 1982 | 1983 |
| 1987 | May 1986 | Nov. 1983 | Nov. 1983 | May 1985 |
| 1,2,4,8 | 1,2,3,4,5,6 | 1 | 1 | 1 |
| 572 Mflops | 133.3 Mflops | 1,710 Mflops | 3,000 Mflops | 1,300 Mflops |
| 4,600 Mflops | 800 Mflops | 1,710 Mflops | 3,000 Mflops | 1,300 Mflops |
| 7 ns | 15 ns | 7 ns (vector)<br>14 ns (scalar) | 4 ns (vector)<br>8 ns (scalar) | 6 ns |
| 1 Gbyte | 0.5 Gbyte | 0.25 Gbyte | 0.5 Gbyte | 1 Gbyte |
| 8 Gbyte | 2 Gbyte | 1 Gbyte | 12 Gbyte | 8 Gbyte |
| 20K gate CMOS (300 ps) | 612/2,360 gate ECL (N/A) | 400/1,500 gate ECL (350 ps) | 2,500/5,000 gate ECL (200 ps)/(250 ps) | 1,000 gate ECL (250 ps) |
| 256K SRAM (35 ns)<br>1M DRAM (150 ns) | NMOS 1M DRAM (80 ns) | 256K SRAM (35 ns) | 256K SRAM bi-CMOS (20 ns)<br>1M MOS DRAM (120 ns)[extended] | 256K MOS SRAM<br>1M MOS DRAM (N/A) |
| 16;— | 16-128;— | 32;— | 64;— | 6;1 |
| 50;— Mbytes/s | 4.5;— Mbytes/s | 3; — Mbytes/s | 4.5;— Mbytes/s | 15.9;1,300 Mbytes/s |
| 1,000;— Mbytes/s | 500;— Mbytes/s | 96;— Mbytes/s | 288;— Mbytes/s | 95.4;1,300 Mbytes/s |
| Nitrogen (77 k) (logic)<br>Freon (memory) | Water (100-132 chips/ thermal cond. module) | Air | Air | Water (logic)<br>Dehydrated air (memory) |
| SYS V, EOS | MVS,VM,A1X/370 | MSP/MVS/XA/UTS/M | N/A | SXOS |
| Fortran 77, C, Cybil<br>Meta assembly | Fortran 77, APL-2 | Fortran 77 | Fortran 77 | Fortran 77 |
| 16 Add<br>16 Integer<br>16 Divide<br>16 Multiply<br>16 Shift<br>16 Logical | 6 Add/sub/logic<br>6 Multiply/div | 4 Multiply<br>4 Divide<br>4 Add/logical<br>4 Mask | 4 Multiply<br>1 Divide<br>4 Add/logical<br>4 FP Multiply<br>4 FP Add | 4 Multiply/div<br>4 Add<br>4 Logical<br>4 Shift |
| 4 Loads and 4 Stores | 6 Loads or 6 Stores (or any comb.) | 2 Loads or 2 Stores or 1 Load, 1 Store (if contiguous data) | 8 Loads or 4 Loads, 4 Stores | 8 Loads and 4 Stores |
| 256 | 16 GP, 4FP | — | — | 128 |
| — | 2K = 8×256 | 16K (dynamically reconfigurable, 64-2,048 elements/vector) | 16K = 32×512 | 16K |
|  | Cache |  |  | Scalar cache |

- direct support for establishing and operating several supercomputer centers for research, teaching, and applications development,
- tax relief or other financial incentives to supercomputer and related manufacturers,
- tax relief or other financial incentives to supercomputer buyers and users,
- increased direct support of related high-risk research, and
- antitrust relief to the functioning of industrial R&D consortia.

(3) Support all technologies needed for the development of supercomputer systems.

(4) Designate a lead organization to coordinate the roles of the many federal agencies that are critically dependent on supercomputer systems.

(5) Establish and extend national performance goals for the development of scientific supercomputer systems well into the 21st century. These long-term goals should reflect the needs of federally sponsored scientific research, both current and projected.

As a readily implementable, specific action that can be taken now, the subcommittee recommends reinstating government procurement procedures that, during the early days of supercomputers, effectively nurtured the growth of the supercomputer industry. These procedures, often referred to as "buy before fly," allowed the federal procurement system to contract for supercomputers still in design.

One positive move since 1983 was made by the National Science Foundation. As a result of a 1982 recommendation by the Lax Committee, NSF established five supercomputer research centers, which are now in operation. Unfortunately, creation of additional centers seems unlikely, and

**Table 2. Vector-architecture supercomputers in design by manufacturer and series, using data for the largest member of the series (all use 64-bit words).**

| | NEC SX-X/SX-3/44<br>(Announced Apr. 1989) | Fujitsu VP2000/VP2600/20<br>(Announced Dec. 1988) | SSI | Cray-3 |
|---|---|---|---|---|
| First installation expected | 1989 | 1990 | 199X | 199X |
| Number of processors | 1,2,4 | 1,2 | 16,32,64 | 16 |
| Peak performance | | | | |
| Per processor | 5.5 Gflops | 2 Gflops | — | 1 Gflops |
| Total peak performance | 22 Gflops | 4 Gflops | — | 16 Gflops |
| Cycle time | 2.9 ns | 4 ns | 2 ns | 2 ns |
| Maximum main memory size | 2/16 Gbyte | 2/8 Gbyte | | |
| Extended memory | | | | |
| Technology | ECL | ECL | | GaAs, ECL |
| Logic (gate delay) | 20,000 gates/chip<br>(70 ps) | 15,000 gates/chip<br>(80 ps) | | 500 gates/chip |
| Main memory | 256K Bi-CMOS<br>SRAM (20ns) | 1M SRAM (35ns) | | MOS |
| Extended memory | 1M DRAM (150ns) | | | |
| I/O | | | | |
| No. paths (total) | 256+48+8 | 16-128 | | |
| Max. data rate path | 3,4.5,6,9/20/100 Mbytes/s | 9 Mbytes/s (optical fiber Fujitsu proprietary) | | |
| Max. aggregate data rate | 1,068 Mbytes/s | 1,000 Mbytes/s | | |
| Cooling | Water (logic)<br>Air (memory) | Water | | |
| Operating system | Super-UX, SXOS | MSP, UTS/M | Unix | Unicos |
| Languages/compilers | Fortran 77/SX<br>C | Fortran | Fortran,C<br>C++ ? | Fortran,C<br>C++ ? |
| Features | 8 Multiply/Shift | Dual scalar/single vector per processor | | |
| Pipes (vector) | 8 Add/Boolean | | | |
| Registers | | | | |
| Scalar | 512 words | | | |
| Vector | 72K words | 16K words | | |
| Other | Cache | | | |

support of the five existing centers — that is, in the manner deemed essential to keep them on the forefront of supercomputer development — will be difficult.

Currently, the overwhelming momentum in this country is to establish computers at the high-end of the spectrum as consisting of numerous processors, which could be used in parallel, each dealing with different portions of the same problem. The system's effective speed is thereby presumed to increase by $n$-fold, where $n$ is the number of processors. It is still true, however, that we have difficulty writing software to effectively take advantage of such systems. The IEEE Scientific Supercomputer Subcommittee is concerned about the inadequacy of the software provided by US supercomputer manufacturers; another report puts the software area into perspective and recommends actions.[1]

The Japanese, our major competitors in supercomputer development, seem less interested in building parallel-processing hardware. Their manufacturers endeavor to build the fastest possible uniprocessors, hoping to place them in parallel structures at a later time. Improvements in basic technology are not coming as fast as they used to, but the Japanese are working at a faster pace in this area of development than we are.

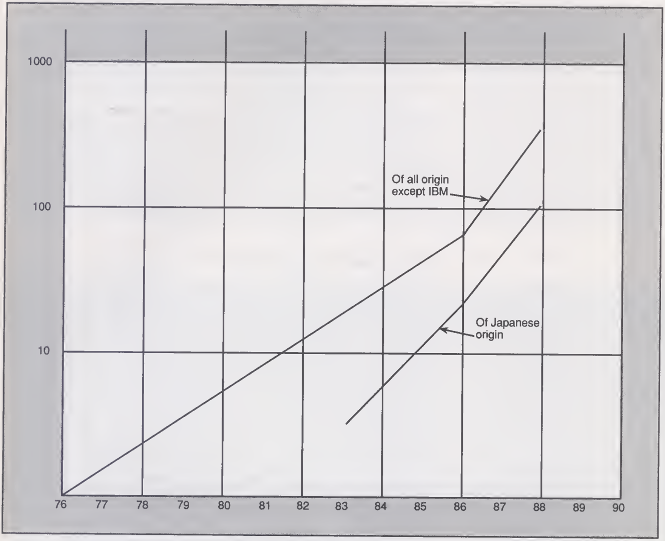
A continuing need in supercomputers is increased, directly addressable memory. This country's semiconductor memory chips come mainly from Japan. The price for these chips is much higher in the US than in Japan, primarily because of Japan's position as the leading producer of semiconductor memory components and our ineffective trade agreements with Japan.

The market for supercomputers has grown significantly since 1983. At that time, 60 had been installed worldwide, mostly in the US and approximately half at

| Cray-4 | Cray C-90 |
|---|---|
| (Early in design process) | |
| 199X | 199X |
| 64 | 16 |
| 2 Gflops | 1 Gflops |
| 128 Gflops | 16 Gflops |
| 1 ns | 4 ns |
| GaAs | |
| Unicos | Unicos |
| Fortran,C<br>C++ ? | Fortran,C<br>C++ ? |

**Table 3. National supercomputer efforts.**

| | Japan | Europe/ESPRIT | |
|---|---|---|---|
| Name | High-Speed Computing | Supernode I; II | Suprenum-ISIS |
| Period | Jan. 1982 - Mar. 1990 | 1984-1988;<br>1988-1992 | 1988-1992 |
| Funding | $140M (Yen 23B) | $25M; $30M | $1.5M Phase 0<br>$40M Total |
| Performance goals | 10 Gflops | 40-1,500 Mflops;<br>200-10,000 Mflops | 40-120 Gflops |
| Current objectives | New devices(JJ,HEMT)<br>Dedicated image-processing system<br>Parallel architectures<br>Parallel algorithms<br>Parallel languages | Parallel processing | |
| Participants | Electrotechnical Laboratory<br>Hitachi<br>Fujitsu<br>NEC | Thom EMI<br>Telmat<br>INMOS<br>RSRE<br>ARSIS<br>Univ. of Grenoble<br>Univ. of Southampton | Germany<br>France |
| Methods for putting results into practice | Incorporated into industrial participants' own supercomputer efforts; special-purpose architecture for a national need | Creation of a new industrial corporation | |



**Cumulative number of supercomputers, 1976-1988. Top line includes supercomputers of all origin except IBM, estimated at 300 by the end of 1988. Note logarithmic scale.**

government sites. As of March 1989, approximately 400 (by Cray, ETA, Fujitsu, Hitachi, and NEC) had been installed, and rapid growth continues, with the greatest rate of growth being in Japan for Japanese-manufactured systems. Tables 1 and 2, updated from the 1983 report, indicate present status (Table 1) and planned activities (Table 2) in industrial supercomputer development. Table 3 addresses European and Japanese efforts aimed at supercomputer hardware and software development; it presents the nature and scope of current national efforts and methods for putting the results into practice. The US has no comparable efforts. Finally, the graph shows the cumulative number of vector-architecture supercomputers.

The OSTP/FCCSET report goes further in its recommendations than the reissued 1983 IEEE report. OSTP considers improvements in networking and long-term support for more basic research in areas affecting future development of supercomputers. The subcommittee wholeheartedly supports these additional activities.

## Reference

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Editor: Fletcher J. Buckley, GESD, MS: 148-304, Moorestown, NJ 08057-0927; phone (609) 866-6350; fax (609) 866-6289; Compmail+ f.buckley

# Some standards for software maintenance

*Fletcher J. Buckley*

Software is rapidly inundating the computer community. Billions of lines have been written, millions more are written every year, and very little of it is discarded. Indeed, the hardware may have been changed, but the software lives on forever.

There appear to be a number of forces at work to keep the old software going:

(1) It works and, in our world, once we have something that works, we think long and hard before trading it in for a promise.

(2) Once we have something that works, the risk in adding more features to it to enhance its operation is minimal.

(3) We have to live with a shortage of competent people and restricted budgets. Rather than redoing software that already works and does at least a part of what we want it to do, we consider it better to live with what we have and apply our limited resources to obtain a new capability.

(4) Finally, few may know the guts of these old software programs, but they work and produce creditable answers. Fear of destroying these old programs causes us to work around them, and the programs live forever.

The result is part of the lore of the field: 50 to 80 percent of the total life-cycle cost of our software is spent on maintenance, repairs, or enhancements. Yet, the bulk of the literature and the majority of the research examines the process of software development while almost ignoring maintenance.

**The need for good documentation.** To maintain the software, we need to understand it. This implies some mechanics of understanding the software's construction, its framework, and its architecture. We need some higher-level view that does not contain all the details in the source-code listings. We need a document that will help a person not familiar with the program quickly grasp an understanding of it. By default, the documentation prepared during software development is usually proposed to provide this higher-level view; for example, the software design documentation. This is sometimes, under various schemes, combined and augmented to produce software maintenance manuals.

This approach has at least two problems:

(1) The design documentation is not kept up to date.

(2) The design documentation is not designed for maintenance.

**The purpose of design documentation.** The primary purpose for design documentation is to create a set of plans for the construction of the software; that is, as a "build to." As such, it usually contains certain things, such as a program design language (PDL), that assist the programmer in writing the source code.

Once the software has been constructed (in the form of code), the design documentation is, in effect, usually abandoned. The reasons for this are quite straightforward. The developer is paid when the system has completed its acceptance test, and the system tests cannot be started until the software tests are completed. Therefore, every person who can help with testing the software is pressed into service.

All those who know the software are involved in supporting the test activities, and no one is left to keep the design documentation up to date. (For those who doubt this scenario, consider the reaction of a project manager on being told that competent, knowledgeable people are available but not being applied to complete the software test activities. This extends the completion date of the system test, with further consequences on other milestones.)

In theory, after the software testing ends, the design documentation is brought up to date before final delivery. What actually may happen is this: since people are scarce and the ones on the project are transferred to the next development, those left to bring the documentation up to date will only be concerned with doing enough to enable them to be transferred to the next development project.

This process is hastened by the roars of the project manager, who wants everyone off the project, the shop orders closed, and the project declared completed. (The process is further encouraged by fixed-price contracting. Every additional dollar spent on documentation is a dollar expended against the fixed-price contract and hence comes out of profit.)

The current response to all this is to have a physical configuration audit as part of the contract. In theory, a complete review will be made of all the software design documentation at that time. Documentation that does not meet standards is then redone and reissued.

In looking at the practice, consider the documentation for one computer program of approximately 30,000 lines of executable source code, approximately 400 source files. The associated documentation will add up to about 1,000 pages of text, tables, and figures, and about 1,000 pages of listings. Going through that much material in some reasonable time period (say 30 days) is a heroic task.

The situation becomes worse when

(1) the standards to which this documentation is to be written are, at best, ambiguous;

(2) the customer's people performing the review are not skilled in the application or the programming language;

(3) the reviewers have other duties (for example, analysis of system test results); and

(4) at least three other computer programs of similar magnitude are also being delivered for review at the same time.

The task is, literally, impossible.

**History repeats itself in the maintenance phase.** Setting all that aside, assume that the design documentation was complete, correct, and current when delivered. Now, those engaged in maintenance are placed in exactly the same turmoil — not enough time, money, or incentive to keep the maintenance documentation up to date — as the developers previously experienced.

Even worse, the design documentation is, in part, redundant with the source code. For example, the PDL mentioned above now appears in both the design documentation and the source file headers. The maintenance programmers must now enter the same information in two different locations.

The upshot of all of this is that, after a year or two, those engaged in fixing bugs and making minor changes will discover that the documentation is not current. The response is to abandon the documentation and revert to the source code listing.

The bottom line is that the need still exists for a higher-level understanding of what the code does. However, the approach of having a separate manually maintained document provide that information is not viable.

When this problem is posed, several solutions are usually projected:

(1) This is transitory and will be overcome by fourth-generation languages. This response fails to solve the real problems of today, the billions of lines of code that already exist in Cobol and Fortran.

(2) Failure by the maintainers to keep the documentation up to date is merely a failure of the will. What we need is more management direction and all will be well. This is an application of the "more" theory; that is, what we have done hasn't worked so we will do more. It does not address the causes of the problems and thus fails to be a workable solution.

The overall result is that, in today's world

(1) Truth is found only in the listing.

(2) The span of understanding for a programmer is from 7,000 to 15,000 lines of source code.

(3) It takes three to six months for a programmer to achieve a good working understanding of that amount of code.

(4) The amount of code to be maintained is rapidly approaching the point where it will consume all the available work force.

**Conceptually simple solution.** The solution to this impasse is conceptually simple. We already have working code in the software maintenance phase of the life cycle, and this contains all the information on the computer program itself. Even better, this situation is deterministic. From this code we could abstract higher-level charts, data, and control flows, etc. These, in turn, can be packaged with templates, style guides, and predetermined formats through the use of some fairly elementary software processes.

The whole process is called "reverse engineering." But, two factors prohibit this from taking place:

(1) We really don't have a good, unambiguous standard for maintenance documentation because we haven't determined what is really needed in the amount of detail required. (Projecting the use of the design documentation implies that the "build to" documentation is what is required to document the "as built" code. This may be a very poor choice.)

(2) Without a good, unambiguous standard for maintenance documentation, there is no incentive for the commercial marketplace to build products that will "reverse engineer" the code to provide the maintenance documentation.

We need a good, unambigious standard for maintenance documentation that then can be produced from the code.

To solve this problem, an IEEE working group is being formed to produce a standard for software maintenance. Those interested in participating in the development of that standard should circle reader service card number 185.

Additional discussion of the problems inherent in software maintenance are provided at two specific conferences on that topic. For information on the IEEE Computer Society Software Maintenance Conference, circle reader service card number 186. For information on the conference sponsored by the Software Maintenance Association, circle reader service card number 187.

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The University of Maryland's Institute for Advanced Computer Studies and Center for Automation Research are soliciting applications from qualified graduate students for research assistantships in parallel processing. These assistantships are made available by funds provided by the Defense Advanced Research Projects Agency's (DARPA) Information Science Technology Office through a contract from NASA Ames Research Center. Proposals can address either fundamental issues in parallel processing (e.g. architectures, algorithms, programming languages, performance evaluation, etc.) or significant applications of parallel processing. Research proposals that have an experimental component will be given highest consideration for funding.

Awards will be made for one year of support, with possible extension to a second year based on progress made during the first year. Funds will be provided as part of the award to the student's university for salary, tuition, and benefits. The University of Maryland will provide direct travel support to an annual workshop held in conjunction with the program at which students will deliver papers describing their research and interact with leading scientists and engineers in parallel processing. If requested, students will be provided with free access to the University of Maryland's Connection Machine II.

Applications are solicited for **June 1990** funding. Only one student per department will be funded.

**_Who Can Apply_**

Applicants must be:

- U.S. citizens and
- doctoral students who have completed all course work and preliminary exam requirements.

**_How to Apply_**

Applications (3 copies) should be submitted to Prof. Larry Davis, Director, UMIACS, University of Maryland, College Park, MD 20742 by **January 26, 1990**. An application consists of:

- a short research proposal (at most 3 single spaced typewritten pages)
- a budget endorsed by an appropriate official at the student's university (The budget should only include salary, tuition, benefits and overhead, if charged.)
- a letter of support from the student's faculty advisor who will serve as principal investigator
- curricula vitae of the student and advisor

**_For Additional Information (contact)_**

Ms. Johanna Weinstein
UMIACS
University of Maryland
College Park, MD 20742-3251
301/454-1808
johanna@umiacs.umd.edu

# Computer Society NEWS

Editor: Guylaine M. Pollock, Sandia National Laboratories, 1424, PO Box 5800, Albuquerque, NM 87185; phone (505) 846-0040; electronic mail: gmpollo@sandia.gov.

## Members urged to nominate others in society for election to IEEE fellow

*Michael C. Mulder, University of Southwestern Louisiana*

One of the goals the IEEE Computer Society set for 1989 was to increase the number of society members elected to the IEEE fellow grade. A small task force is now making a concerted effort to see that at least 100 worthy Computer Society candidates are nominated for fellow by the next deadline.

The society's record in the IEEE fellow area has not been very good in the recent past. For instance:

- About 400 IEEE fellow nominations are submitted each year.
- Typically, 55 percent of those nominated are elected (in 1988, 226 or 57 percent were elected).
- In 1988, however, only 38 of the 226 elected were Computer Society members.
- The figures cited are disturbing because the Computer Society represents approximately 45 percent of the IEEE membership. It appears the society is underrepresented in this important area of professional recognition.
- Of even more concern is the fact that, of the 38 Computer Society members elected, only 18 were nominated by others in the society.

**Action needs to be taken.** In this regard, the society clearly has a problem. Since the title of fellow is reserved for those who have contributed significantly to our profession in truly outstanding ways, the society's low representation at the fellow grade is not representative of its technical, educational, and leadership contributions to its profession.

We have many colleagues who are worthy of fellow recognition. We need to encourage our peers to get involved in the nomination and support process for those who should be recognized through this prestigious election. Therefore, we request that you, as Computer Society members, take the initiative to identify peers who deserve fellow recognition and lead the nomination process.

In hopes of reaching the aforementioned goal of nominating at least 100 deserving Computer Society candidates for fellow, society President Ken Anderson has created the small task force I am heading to encourage and assist more fellow grade nominations from our membership. Once a candidate is nominated, the Computer Society Fellows Committee chaired by Tilak Agerwala will complete the society's part of the nomination process.

Each fellow nominee must

- be an IEEE senior member;
- demonstrate significant individual contribution(s) as an engineer or scientist, technical leader, or educator;
- provide tangible and verifiable evidence of contribution(s);
- have the Computer Society Fellows Committee's endorsement;
- receive confidential recommendations by five other IEEE fellows; and
- show evidence of IEEE service.

Once the nominee is identified, the three following applications forms must be filled out in his or her behalf (the forms are now available from the Computer Society and can also be obtained from Mulder or Agerwala at the addresses below):

- Fellow Grade Nomination Form (B-27), to be completed by the nominator.
- Fellow Grade Reference Form (B-29), to be completed by five IEEE Fellows.
- Computer Society Evaluation (B-3), to be completed by the Computer Society Fellows Committee.

The nominator — the member who as-

## *IEEE Computing Futures* pilot published

A new, experimental student publication, *IEEE Computing Futures*, is being published this month.

Subtitled "By and for the IEEE Computer Society Students in Central and Northern California," the 86-page publication was conceived, proposed, developed, and refereed by a nucleus of IEEE-CS student chapter activists led by Ben Chang, now a Stanford University graduate student, and Darius Wallace, who now works at Amdahl. Chang and Wallace originally proposed the idea to chapter advisor C.V. Ramamoorthy in 1988 when both were still undergraduates at UC Berkeley.

Professor Ramamoorthy reviewed the idea with then-President Ed Parrish and brought it forward to the Publications Board's Planning Meeting, held last January. In March, Chang and Wallace formally presented their proposal to the Publications Board, where the concept was endorsed to produce a pilot issue under the guidance of Vice President for Education Gerald L. Engel.

According to Ramamoorthy, the publication answers a need for technical communications among computer science and engineering students that is not presently being met by individual student chapters, by *Computer*, or by *IEEE Potentials*. It permits leaders from several student chapters in a geographical area to organize and work toward a common, worthwhile goal.

*IEEE Computing Futures* will feature interviews with Andy Grove of Intel and Bob Maxfield, a co-founder of Rolm, plus technical articles on AI, fault tolerance, DBMS, computer networks, a content-addressable memory-based search accelerator, bubble memories, cellular automata, and image compression. Other features include a personal profile, a student account of Pacific Bell's summer program, and profiles of several universities in Central and Northern California.

*IEEE Computing Futures* is being distributed as a demographic supplement to this issue of *Computer* to all IEEE-CS student chapters in Central and Northern California and to *Computer* library subscribers. While supplies last, it is available to other IEEE-CS student chapters on request.

sumes the leadership role in getting the forms completed and sent to the IEEE Fellow Committee — is the key to a successful nomination.

**Nomination package available.** If you would like to nominate a worthy candidate, contact Michael C. Mulder, Center for Advanced Computer Studies, University of Southwestern Louisiana, PO Box 44330, Lafayette, LA 70504, phone (318) 231-6147, e-mail mulder@usl.usl.edu, Compmail+ m.mulder; or Tilak Agerwala, IBM, 11400 Burnet Road, Austin, TX 78758, phone (512) 823-6870.

The completed nominations should be sent directly to the IEEE Fellow Committee at IEEE Headquarters by April 30, 1990.

We on the ad hoc task force hope that you will get involved in this process to achieve our goal of nominating at least 100 candidates from the Computer Society. Please help us make this effort a success.

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# Packaging TC tackles problems through workshops, investigations

*John W. Balde, Vice Chair, Liaison, Computer Packaging Technical Committee*

Composed of highly active national and international researchers, the IEEE Computer Society's Computer Packaging Technical Committee has strived for 23 years to advance innovative research in the computer packaging industry.

To meet that objective, the TC sponsors four technical workshops each year and coordinates investigative ad hoc task forces made up of researchers from different companies. The TC meets five times a year to oversee the workshop and task force efforts.

The TC was organized in 1966 as a spin-off of the Computer Elements Technical Committee. It confines its attention to issues linked to the physical design of computers and computer-related systems.

Because of the TC's long history, members have been leaders in the formation or organization of other societies focusing on packaging and are very active within this industry. For example, several members were among the founders of the International Electronic Packaging Society (IEPS). In addition, members of the TC serve on the advisory board and chair sessions for Nepcon (the National Electronic Packaging and Procedures Conference) and serve on committees for the VLSI and GaAs Workshop and the IEEE Components, Hybrids, and Manufacturing Technology Society's (CHMT) International Electronic Manufacture Technology Conference (IEMT).

**Technical workshops.** The TC's sponsorship and support of technical workshops allow its membership to maintain their leadership in advancing the state of the art in computer packaging. Workshop attendence is by invitation and limited to 100 people, generally on a first-come basis but with limitations on the attendees from any one company to ensure a mixed audience and to avoid domination by a group of "regulars." Invitations are only sent to those members who have attended TC meetings within the previous 24 months.

The Split Rock Workshop, the original computer packaging workshop the TC organized, has been held in the Pocono Mountains every other year since 1968. The May workshops feature five technical sessions over a three-day period. Two evening sessions are held. Attendees have represented the US, Japan, Canada, and Europe.

Due to the success of the first workshop series, attendees from US West Coast companies organized a set of workshops for that region that are held during alternate years from the Pocono Split Rock Workshops. Hosted in various locations in May, the West Coast workshops have also proved highly successful. Past sessions have been held in such California cities as San Diego, Monterey, Palm Desert, Solvang, and Santa Cruz.

Two other packaging workshops have borrowed the successful Split Rock and West Coast workshop format and structure and are conducted in alternating Januarys outside the US.

Two workshops have been organized in Oiso, a resort seaside town near Tokyo, and a third is planned there. These workshops are administered by a Japanese committee, which is solely responsible for the programming. The Oiso workshops have been successful, in both content and attendance.

The fourth workshop series is held in Europe, thus providing a more local venue for those in the packaging fraternity on that continent. Attendance has been near the limit. The two European workshops held to date were conducted in Brussels, although a different city could be selected for a future event.

This schedule of two workshops a year, in the Poconos and Oiso in even years and California and Brussels in odd years, seems to be the most that can be sustained without exhausting the supply of innovative papers and speakers. Because these workshops do not produce publications, the material content is usually six to nine months in advance of any available publications — one of the major attractions of workshop attendance.

To maintain active sponsorship of the workshops, the TC conducts meetings almost every other month. The committee generally meets at IEEE Headquarters in New York, although occasional meetings are held elsewhere at the invitation of an electronics or computer manufacturer that provides the necessary space and offers tours of their facilities or laboratories.

Attendance at these meetings is open to anyone interested in computer packaging issues. However, mailing lists for the meetings are reduced each year to active participants, and names are not added to the list until there is attendance at some meeting.

**Task forces organized.** Since 1975, the TC has organized ad hoc task-force efforts to solve industrywide problems that require intercompany cooperation.

Through previously conducted investigations, one task force promoted standardization of the chip carrier package type, and another task force promoted standardization and acceptance of under-carpet wiring for power, telecommunication, and data. Both investigations were highly successful, with the Chip Carrier Task Force relegating the issuance of standards to the Joint Electron Devices Engineering Council (JEDEC) and the Under-carpet Wiring Task Force providing substantial input to the National Electric Code and to subsequent standards published by the Institute for Interconnection and Packaging of Electronic Circuits (IPC).

Current TC-sponsored efforts include the Compliant Lead Task Force and the IEEE Gel Task Force. Both investigations are nearing completion, and final reports are expected in 1990.

The Compliant Lead Task Force has completed an investigation of the dependence of the reliability and life expectations of soldered "J" leaded chip carriers. The investigation has determined that major differences in the probable performance life depend on the material, the shape, and the length of the leads used in developing chip carriers. Some of the industry packages are clearly little better than leadless carriers, while others add greatly to probable life.

The task force will make available its design of an isothermal bending fixture for 12 boards and the specifications of the testing procedure, in addition to a final report. The IPC and IEEE Electronics Components Conference (ECC) have published Figures of Merit data, presentations built on the results from this task force activity, and presented information on the expected life of soldered "J" leaded chip carriers for various applications.

The IEEE Gel Task Force is focused on establishing that one of the surface coatings of silicon gel is able to provide semiconductor die protection equivalent to that provided by the use of hermetic ceramic packages. Results from testing 600 packages are expected to be presented by the end of the year. The task force will also publish the specification for the thermal shock, salt spray, and autoclave testing used to determine the reliability.

Other TC task forces will be established from time to time. The next one is expected to be in the area of standardization of multichip module packages.

Although the task forces sponsored by the TC tend to provide significant input to standards in the computer packaging area, they do not develop actual industry standards. They organize a general consensus and then turn the standardization activity over to other on-going standards organizations. However, the task forces do publish test methods, if test programs are used, so that their testing methods can be used throughout the industry to permit gathering of comparable results. While these methods may become de facto standard test procedures, no decree or force of organization ruling exists that requires their use; that requirement is left to other organizations — such as the IPC or RADC (Rome Air Development Center) — that develop actual standards.

TC **adminstration.** A steering committee, consisting of TC members who have chaired technical sessions at monthly meetings or at workshops, administers the TC. There is no designated succession ladder, although the past chair is always the new vice chair to ensure that an experienced individual is on hand to preside should job demands make the chair unvailable.

The TC receives no funding from the IEEE. It operates on a break-even basis and makes all arrangements with volunteer help and no professional assistance. It does not sponsor conferences or issue publications, transactions, or quarterly newsletters.

The IEEE Components, Hybrids, and Manufacturing Technology Society acts as the publication service for the TC. Since this relationship was established in 1980, computer packaging papers have been published either once a year or every 18 months as part of a special section in *IEEE CHMT Transactions*. The section is organized by a Computer Packaging TC representative serving as guest editor.

Marty Freedman of AMP is the current TC chair, with Gene Shapiro, IBM, the vice chair; John W. Balde, IDC, the vice chair, liaison; and Art Murphy, Dupont, the treasurer. Teruo Murase, Fujitsu, chairs the Japan Committee; and Maurice Sage, BPA, chairs the European workshop. Interested Computer Society members may contact them for further information about the TC and its activities. Balde may be reached by phone at (201) 788-5190.

In order, the former committee chairs since 1966 were Bob McMahon, Massachusetts Institute of Technology; Bert Walker, RCA; Jack Rausch, Bell Laboratories; Balde; Tony Close, Bell Labs; Don Franck, IBM; Tom Matcovich, Drexel; Walt Vilkelis, IBM; Dan Amey, Univac; Wulf Knausenberger, AT&T, and Shapiro. Ray Usell of Unisys and Paul Wesling of Tandem have headed West Coast activities; Makoto Watanabe of NTT and Hisao Kanai of NEC, the Japan Committee; and Sage has organized the European workshops.

# TC Microprogramming member interests tend toward microarchitecture

*Yashwant K. Malaiya, Chair, Technical Committee on Microprogramming*

IEEE Computer Society members first became highly interested in microprogramming during the 1960s. At that time, the flexibility Wilkes' scheme offered for implementing the control unit became apparent. This growing interest led to the formation of the Technical Committee on Microprogramming.

In a narrow sense, the term microprogramming refers to a systematic technique for implementing a desired instruction set. However, members of TC Micro are interested in all aspects of processor design.

The TC's worldwide membership represents both industry and academia. Recent technological advances have removed many of the obstacles that restricted designers in the past. There is a considerable resurgence of interest in this field. Some of the widely different approaches being used or investigated today were considered infeasible or speculative only a few years ago.

The term microarchitecture perhaps describes the interests of TC Micro more comprehensively. This term describes a view at or near the micro-operation level. It views the architecture above the gate level but below the system level — that is, where the interaction of hardware and software is most apparent.

**Major activity.** Together with ACM's SIGMicro, TC Micro sponsors Micro-*n*, the Annual International Workshop on Microprogramming and Microarchitecture. Micro 1, the first in the series, was held in 1968. Although Micro-*n* is termed a workshop for historical reasons, proceedings have been published every year for almost two decades, and the papers are refereed.

To promote an uninhibited exchange of ideas, the informal character of the working group discussions has been carefully preserved. The prospective attendees are even encouraged to leave their ties at home.

In 1988, Micro-*n* was held in San Diego and chaired by Yale Patt of the University of California at Berkeley, with Wen-Mei Hwu of the University of Illinois at Urbana-Champaign the program chair.

This year's workshop, Micro 22, was held in August on the historic campus of Trinity College in Dublin, Ireland. The general and program chairs were Gerry Johnson of Colorado State University and Bob Mueller of QTC, respectively. The 31 papers selected for presentation represented authors in North and South America, Europe, Asia, and Australia.

**TC reorganized.** In the past several years, the discipline of processor design has changed radically. What once was considered settled, has begun to be questioned widely. Now, the concepts of RISC (reduced instruction set computing) and extensive pipelining have been accepted, and it has become both feasible and cost-effective to manufacture special-purpose processors for graphics, signal processing, and other applications. Furthermore, VLIW (very long instruction word) architectures are attracting serious attention.

It was once thought that automation could only be successfully used at the gate and lower levels. Today, we're seeing a shift towards higher level building blocks. As a result, design automation at the micro-operation, or even higher, levels has also received considerable attention.

These changes in the focus of recent research efforts have led to a reorganization of TC Micro to provide a wider scope that will address changing issues of interest to its membership.

Current topics of interest to the membership include

- Microarchitecture models: control, data.
- Microarchitecture implementations: hardware, software, firmware.
- Evaluation of microarchitectures: performance, timing, overhead, testability, etc.
- Architectural variations: parallelism, pipelining, RISC, CISC, dynamic microprogramming, etc.
- Application-oriented architectures: graphics, data acquisition, signal processing, high-level languages, etc.
- Design tools: microprogramming languages, microcode compilers, simulators, evaluation systems, RTL (register transfer language)-level techniques, rapid prototyping, emulation, etc.
- Hardware: programmable logic, bit-sliced and functionally partitioned devices, library cells, controllers.
- Design optimization: microcode compaction, encoding, layouts.
- Testing: concurrent testing, testable design, functional testing, timing, microcode verification.

TC Micro has set the following goals for the next several years:

- Expand the areas of interest to include all aspects of computer microarchitecture.
- Increase the number of active participants in the US and abroad.
- Initiate awards to recognize curriculum and lab development efforts.
- Develop Micro-*n* into a major international symposium maintaining the current trend.
- Initiate a new international workshop on automation tools for high-performance processors. (The society's TC on Design Automation plus ACM's SIGDA and SIGMicro have shown interest in cosponsoring such a meeting. This workshop will have an informal format to allow all attendees to actively participate.)

**Publication launched.** The TC has initiated a new publication called *MicroArch* that is eventually expected to become a quarterly. Each issue contains not only news, announcements, and comments but a few short original technical articles.

The publication exploits the current technology (widespread availability of typesetting software, electronic mail, and laser printers) to quickly disseminate ideas in a very clean and readable form that approaches the quality of professionally typeset publications. All members of TC Micro, both in the US and overseas, receive *MicroArch* free of charge.

Today, some major journals take as long as three years to publish a paper. Some major conferences in this and related areas now can only accept 20 to 30 percent of the papers submitted. *MicroArch*, thus, provides a significant service by allowing fast dissemination of evolving or speculative ideas. Depending on the availability, back issues may be obtained by contacting the editor.

**Committee leadership.** The current TC Micro office holders and the area of their recent contributions in this field are as follows:

*Executive Committee:* Yashwant K. Malaiya, chair (Colorado State University), choices in control architectures; Robert A. Mueller (QTC), retargetable microcode compilation; Larry Kinney (University of Minnesota), concurrent testing; and Christos Papachristou (Case Western Reserve), test scheduling and pipelining.

*Advisory Committee:* Alice Parker (USC), high-level synthesis; Stanley Habib (City University of New York), description languages; Michael Andrews (Space Technology Inc.), firmware engineering; Joseph Lynn (IDA), microcode compaction; and Bogong Su (University of Beijing), code optimization.

*Editorial Board,* MicroArch: Yashwant K. Malaiya, editor, and Anura P. Jayasumana (Colorado State University), associate editor for VLSI and design automation.

TC Micro's chairs over the years have included several distinguished researchers. Bruce Shriver, the editor-in-chief of *Computer*, led TC Micro in 1981-82. Scott Davidson, supervisor of the automatic test generation group at Bell Laboratories in Princeton, N.J., chaired TC Micro the next two years. Joseph Lynn was the chair in 1985-87.

TC Micro is an open organization, meaning anyone interested may join. There is no membership fee. Volunteers are invited to assist in our activities.

For further information, contact Yashwant K. Malaiya, Computer Science Department, Colorado State University, Fort Collins, CO 80523, phone (303) 491-7031.

## Society plans computer bridge contest

Contestants are invited to develop bridge-playing programs and enter a computer bridge contest sponsored by the IEEE Computer Society. It will be held in conjunction with the Sixth IEEE Conference on Artificial Intelligence Applications March 7-9 in Santa Barbara, California.

The tournament will be divided into bidding and play, but programs need not participate in both categories. Only the Standard American/2 over 1, ACOL, Kaplan-Sheinwold, and Precision bidding systems will be allowed. International Matchpoint (IMP) scoring will be used.

An independent computer will be used to simulate each "player." The tournament will be conducted as a Swiss team event. Programs will bid/play the same hand twice against each other with the north/south and east/west positions reversed.

Each team will need two portable computers to simulate the players.

There will be no entry fees, but players must sign up by February 1, 1990. To enter or obtain more information, contact Willis K. King, Department of Computer Science, University of Houston, Houston, TX 77204-3475, phone (713) 749-4791, e-mail wkking@cs.uh.edu.

# UPDATE

Contributions to Update are welcome. Send news of industrial or university research and of public policy or professional issues to Update Editor, 10662 Los Vaqueros Circle, Los Alamitos, CA 90720, or to Editor-in-Chief Bruce D. Shriver, Vice President for Research, University of Southwestern Louisiana, Drawer 42730, Lafayette, LA 70504.

## High-performance computing suddenly high profile

*Steve Wilcox, Staff Editor*

The White House and the US Congress are again spotlighting proposals to spur US development of high-performance computing resources, two years after a White House report called for a long-range strategy.

In September, the White House's Office of Science and Technology Policy issued *The Federal High-Performance Computing Program*, a detailed program plan called for in the office's 1987 report.

Earlier in the year, Sen. Albert Gore, Jr., of Tennessee introduced Senate bill 1067, the National High-Performance Computer Technology Act of 1989, to "ensure continued United States leadership in high-performance computing." Rep. Doug Walgren of Pennsylvania introduced the same legislation as House bill 3131.

The White House plan contains four components: hardware and system software; software technology and algorithms; a proposed National Research and Education Network; and basic research and human resources.

In the basic research component, goals include attaining an annual level of 1,000 computer science PhDs by 1995, upgrading 10 university computer science departments to the standards of the 10 best departments, and upgrading an additional 25 departments to "nationally competitive quality."

The report's recommendations for high-performance hardware and system software would require $680 million above current funding levels over five years, software technology and algorithms would need $660 million, NREN would need $390 million, and basic research and human resources would require $183 million. The first three components would also set aside 15 percent of their budgets for basic research. Also, the budget for the software component includes $153 million for work on fundamental scientific problems identified as "grand challenges," including semiconductor design, superconductivity, speech understanding by computers, weather prediction, and quantum chromodynamics.

Although the Office of Science and Technology Policy would manage the proposed program, individual agencies would need to define their own goals. Each agency would also provide its share of the necessary funding from its own budget. The four main funding agencies now spend about $500 million annually on related projects. The first year of the proposed plan would require an additional $150 million. By the program's fifth year, annual funding would be about $600 million above the current level.

> **"A future national high-speed network could have the kind of catalytic effect on our society, industries, and universities that the telephone system has had during the 20th century."**
>
> *— D. Allan Bromley, director of the Office of Science and Technology Policy*

The White House report stresses that the document is "designed for agency-level planning purposes" only. President George Bush's budget proposals do not include the recommended funds.

**NREN.** The proposed National Research and Education Network has received by far the most public attention. A high-speed network linking researchers across scientific disciplines and providing access to supercomputers "could have the kind of catalytic effect on our society, industries, and universities that the telephone system has had during the 20th century," said D. Allan Bromley, director of the Office of Science and Technology Policy, in a letter accompanying the report.

The report recommends that development of NREN proceed in three stages:

(1) Upgrade Internet trunks to handle data rates of 1.5 Mbits/s.

(2) Construct a 45-Mbit/s "shared backbone network" to 200-300 research sites.

(3) Offer networking at speeds from 1-3 Gbits/s to selected research facilities and expand 45-Mbit/s capability to about 1,000 research sites.

The five-year report does not list funding levels for actual deployment of the gigabit network or for its recommended transferal to a commercial service, both of which would occur sometime after 1993.

The congressional bills share many of the White House report's goals, including development of NREN. The legislation would approve $400 million over five years for the National Science Foundation to develop and implement the high-speed network, $750 million for software research and development, $450 million for computer systems, and $150 million for basic research and education.

In addition, the bills would require the NSF to "ensure that the national supercomputer centers . . . have the most advanced, commercially available supercomputers produced by United States manufacturers." The NSF would also be called on to establish software clearinghouses to "validate and distribute unclassified software developed by federally funded researchers and other software in the public domain."

The bills also would require the Commerce Dept. to "review export controls that hinder the development of foreign markets" for US supercomputer manufacturers.

This month's President's Message by Edward A. Parrish, Jr., also addresses the National Research and Education Network. See p. 5.

# Major changes in federal software policy urged

*Galen Gruman, Staff Editor,* IEEE Software

"Government policies on everything from budgeting to intellectual property rights have congealed over time in a manner almost perfectly designed to thwart the development of quality software," concluded a US congressional subcommittee's staff report on federal software procurement and development.

The 35-page report *Bugs in the Program* outlines software-development problems and recommends congressional action to improve federal acquisition and development. The report, which will be publicly available this month, was researched for two years and written by staff members at the House Committee on Science, Space, and Technology's subcommittee on investigation and oversight.

"What has become apparent is that system costs are driven not by hardware but by software," states the report. In 1985, software development accounted for about 40 percent of a system, software maintenance 45 percent, and hardware 15 percent, the report says, quoting Barry Boehm's book *Software-Engineering Economics* (Prentice-Hall, 1981).

The report makes these key recommendations:

- Establish a permanent software-policy apparatus, most likely under the White House's Office of Science and Technology Policy, to raise the profile of software issues and educate government agencies.
- Expand the Software Engineering Institute's role beyond the Defense Dept. or establish similar organizations for other federal agencies.
- Establish a group within the National Institute of Standards and Technology to evaluate development methods before they are introduced into federal agencies.
- Spend more money on development up front, including funds for experiments between competing alternatives, to save money over the project's life.
- Require hazard analysis, particularly for software, during the certification of safety-critical devices.
- Eradicate the waterfall model of development from federal standards. Promote evolutionary development models.
- Give program managers the flexibility to make decisions on software development as it progresses.
- Restructure salaries to attract and keep software engineers in federal agencies.
- Focus research and management efforts on ensuring reliability, safety, security, and quality.

The report also suggests that the government study whether software engineering should be a separate discipline from computer science, and recommends that the profession establish some certification, accreditation, or other basis on which customers like the government could evaluate a practitioner's software-engineering abilities, especially for safety- and relibility-critical systems.

**Procurement.** "The strange policy where the government pays twice for a system — once to buy it and once again to make it work the way it was expected — cannot be sustained in an era of multibillion-dollar shortfalls in the treasury," the report says.

The procurement system forces program managers to write detailed specifications for systems whose boundaries are fluid, does not let them reflect what users have learned, and makes them move to production before answering all questions about how the system will ultimately perform, states the transmittal letter accompanying the report.

Also, procurement guidelines often forbid evolutionary development models. The waterfall design model requires a "legally binding contract specifying in excruciating detail exactly how the system will look at delivery some years hence," the report said, so that changes during development hurt software quality and increase development costs.

**Personnel.** Federal agencies increasingly need well-trained software specialists but cannot offer competitive salaries. Entry-level salaries for computer specialists were 22.7 to 31.6 percent less than in private industry, the report said. Experienced senior managers make 65 percent less than their industry counterparts.

Furthermore, most managers have no technical background. At the Defense Dept., "whether the officer involved has technical expertise applicable to the program he is assigned to manage is a secondary consideration," the report said.

**Technology transfer.** "Many federal agencies have already worked through the pitfalls of increasing complexity in software, but other agencies are not benefiting from that experience," it said. Because technology transfer "requires direct contact between technical professionals," the report urged the Office of Science and Technology Policy to oversee a program of long-term interagency coordination and cooperation in software.

**Education.** The report acknowledged an Association of Computing Machinery report that recommended treating software engineering as a subarea of computer science, not a separate discipline. "On the other hand," the report said, "there may be some benefit to a more focused software-engineering curriculum, especially in supplying critical skills now woefully short in the federal government."

**Accreditation and licensing.** After conducting hearings on integrity in scientific research, the subcommittee for whom the report was written concluded that "a professional community should be permitted to enforce its own standards, so long as it demonstrates a fair, impartial, and expeditious consideration of these questions," the report said. But "failure of the software community to accept [its] responsibility in this area may lead to the loss of [its] prized autonomy," it said.

# Bitnet, CSnet merge, keep networks separate

Two of the nation's leading academic and research computer networks have merged but will continue to maintain physically separate networks.

Educom and the University Corporation for Atmospheric Research, parent companies of the Bitnet and CSnet networks, finalized merger plans Sept. 18. Rather than create a new corporation, the networks elected a new board composed of directors from Bitnet, Inc., and UCAR. New bylaws were also approved. Bitnet, Inc., has been renamed the Corporation for Research and Educational Networking.

The Bitnet and CSnet networks will continue to operate as separate networks. There are no plans to physically merge the networks, said Jim Conklin, Bitnet's director. Except for consolidated billing, users should see no immediate changes, he said. In the next year, users will see gradual improvements in both networks and more information posted about each other.

The corporation will next name working committees to look at joint services, which might include user directories, Conklin said.

— *G. Gruman*

# Kilby and Noyce receive top engineering award

The National Academy of Engineering has awarded the first international Charles Stark Draper Prize to Jack S. Kilby and Robert N. Noyce, independent coinventors of the monolithic integrated circuit, better known as the semiconductor microchip. Each will receive a gold medal at a ceremony in February and will share the $350,000 award. The cash award is the largest given exclusively for engineering achievement.

The NAE also presented the prize to Kilby and Noyce in recognition of their work to bring the IC into successful commercial production and application.

"Very few things have changed the world as dramatically as the integrated circuit," said Robert M. White, president of the National Academy of Engineering, in a prepared statement announcing the award. "The development of the integrated circuit was the single most important event that helped usher in the Information Age. Like the invention of the telephone, the light bulb, or the automobile, the creation and widespread practical application of the integrated circuit has fundamentally changed our lives."

Kilby became an independent consultant in Dallas in 1970, following a 12-year career at Texas Instruments. He led the development of the first computer to use integrated circuits and that of a family of integrated circuits for the improved Minuteman missile, the first military system to use ICs. He also coinvented the hand-held, solid-state calculator and invented the semiconductor gate array.

Noyce is president and chief executive officer of Sematech in Austin, Texas. In 1957 he cofounded Fairchild Semiconductor, and in 1968 he cofounded Intel Corp., the first company to produce high-density memory components and microprocessors. He was Intel's president from 1968 to 1975, chairman of the board from 1975 to 1979, and vice chairman from 1979 to the present.

Kilby and Noyce were chosen by a 13-member committee of engineers from industry, government and academe. Robert C. Seamans, Jr., senior lecturer at the Massachusetts Institute of Technology, chaired the committee.

The NAE established the Draper Prize in 1988 to honor individuals who have contributed significantly to the advancement of engineering and whose achievements have produced important benefits to the "well-being and freedom of all humanity." The prize will be awarded every two years.

## NANYANG TECHNOLOGICAL INSTITUTE

Singapore

(To be reconstituted and renamed the Nanyang Technological University in 1991)

## TEACHING APPOINTMENTS

The Nanyang Technological Institute, fully supported by the Government of Singapore, is one of the two institutions in the Republic that provide education at university level.

Due to our rapid expansion programme and our aim to meet the staff/student ratio of 1:10 speedily, we are presently recruiting staff especially those who specialise in the following areas:

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6. **Programming and Data Structures**
7. **Microprocessors and Microcomputer Systems Design**
8. **Data Communications/Computer Networks**
9. **Database Systems**
10. **Computer Applications**

### SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

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2. **Computer Communications Networking**
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4. **Artificial Intelligence and Expert Systems**
5. **Microelectronics**
   - **- Thick and Thin Film Technology**
   - **- Optoelectronics**
   - **- VLSI**
6. **Communication Networks, Systems and Software**
7. **Digital Signal Processing including Image and Speech**
8. **Power Electronics and Drives**
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| | | | |
|---|---|---|---|
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(US$1.00 = S$1.90 approximately)

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**NANYANG AVENUE, SINGAPORE 2263**

giving their curriculum vitae and the names and addresses of three referees

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Authors should send four copies of complete paper (not to exceed 15 single spaced pages) to Technical Co-Chair:

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University of California, Irvine
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Irvine, CA 92717
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**Papers must be received by January 15, 1990.** Notification of review decisions will be mailed by February 15, 1990. Laser ready papers are due March 15, 1990. Conference proceedings will be available at the symposium. The conference is sponsored by the Orange County chapter of the IEEE Computer Society.

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# PRODUCT REVIEWS

Editor: Richard Eckhouse, UMASS-Boston, Harbor Campus, Boston, MA 02125, Compmail+, r.eckhouse; Bitnet, eckhouse@umbsky, Compuserve, 70516,556

## Versatile storage and file sharing

In the highly competitive mass storage device market, technology improvements over the past few years have provided larger storage capacities, faster performance, smaller drive form factors, and lower prices. Iomega has responded to each of these challenges with their Bernoulli "family" offerings. The latest Bernoulli drives store more data, can access it quicker, use a smaller form factor, and cost much less than earlier models. The company does not intend them to compete directly with nonremovable hard disks, which you can still purchase for less. But in many situations where you need the Bernoulli advantages — removable media, virtual storage capacity, built-in backup, and ruggedness — you can easily justify the extra cost.

This review evaluates the latest Iomega Bernoulli (Bernoulli II) drive products for three popular PC environments: the IBM PC-AT compatible bus (Compaq Deskpro 386), the IBM Micro Channel bus (IBM PS/2 Model 80-111), and the Apple Macintosh (Mac Plus), with special emphasis on data file interchange among the systems. The latest Bernoulli II drives use a 5.25-inch half-height form factor, store either 21 or 44 Mbytes, and are available for single or dual, internal or external mounting. The review units provided by Iomega were all 21-Mbyte drives.

### Bernoulli drive technology

Iomega rates the 5.25-inch Bernoulli drive at an average access time (including settling time) of 40 ms. The data transfer rate (drive to controller) is 5.33 Mbits per second. New caching software (first available with the new 44-Mbyte drives) further reduces the "effective" access time to 24 ms — not the best performance when stacked up against the fastest hard disks, but certainly acceptable.

A tabular view of drive configurations, in chronological order, gives an overview of Bernoulli box and drive evolution. Table 1 shows the basic drive types. The "Drive Configurations" columns show the PC mounting availability of each drive. The single- and dual-drive mountings come in an external Bernoulli Box. The internal drive mounts in a PC or PS/2 disk drive slot and is referred to simply as a Bernoulli Drive II. Generally, the 8-inch drives have an Alpha designation (such as Alpha 10, Alpha 20), and the 5.25-inch drives have a Beta designation (such as Beta 5, Beta 20). The table does not show any special mounting configurations offered, such as the Bernoulli Box Plus (two 8-inch, 21-Mbyte cartridge drives plus an 80-Mbyte hard disk in an external chassis).

Iomega has maintained what I refer to as upward, read-only compatibility within a drive size. For example, cartridges recorded on the 8-inch, 10-Mbyte drives can be read on a 20-Mbyte drive, but you can't record on a 10-Mbyte cartridge in a 20-Mbyte drive. This means that when you upgrade to a higher capacity system, you must transfer your data to new cartridges if you need both read and write access.

The interface boards and software have also improved with each new configuration. A host adapter board plugs into a PC or PS/2 expansion slot to provide the SCSI interface. Two board variations are available for each bus, nonbootable and bootable. The bootable card includes a ROM and additional chips that allow you to configure the system to boot from a cartridge, just as though it were a hard disk.

Iomega's utility software (always good) has come a long way since the early days. The version I tested, 4.60, worked flawlessly with both the old and new drives. Other than the device driver, it is all menu driven and very easy to use. It also has been upgraded for compatibility with DOS 4.0.

The standard basic software is now referred to as the RCD (Removable Cartridge Disk) System. In addition to these RCD utilities, the setup program included greatly simplifies installation, and a diagnostic program (RCDdiag) comprehensively tests the Bernoulli system's health and configuration status.

RCDdiag is great — the kind of program that can save you hours during problem analysis. It helps diagnose operating problems and can even identify host adapter board switch and jumper settings with the board still in the computer. The RCDdiag main menu shows information on the host adapter board, the Bernoulli (RCD) drives, the RCD device driver, and the boot ROM on the host adapter board. When you see detailed information on the Bernoulli drives, you can run a nondestructive diagnostic test on the selected drives. Each menu item can be retested. When errors occur, the RCDdiag screen displays an error code and corrective-action information.

**Table 1. Bernoulli Box configurations.**

| | | | Drive Configurations | | | Systems | | |
|---|---|---|---|---|---|---|---|---|
| Cartridge Size | Capacity | Form Factor | Single | Dual | Internal | PC | PS/2 | Mac |
| 8 inches | 10 Mbytes | Full height | Yes | Yes | No | Yes | No | No |
| 8 inches | 10 Mbytes | Half height | Yes | Yes | No | Yes | No | Yes |
| 8 inches | 21 Mbytes | Half height | Yes | Yes | No | Yes | Yes | Yes |
| 5.25 inches | 5 Mbytes | Full height | Yes | Yes | No | No | No | Yes |
| 5.25 inches | 21 Mbytes | Half height | Yes | Yes | Yes | Yes | Yes | Yes |
| 5.25 inches | 44 Mbytes | Half height | Yes | Yes | Yes | Yes | Yes | Yes |

## Hardware installation

Installing a Bernoulli system is easy. Iomega's documentation and supporting software make the process almost idiot proof. The basic steps for PC or PS/2 systems are (1) install the host adapter board (and drives), (2) connect the Bernoulli Box (or drives), and (3) install the Iomega software. The IBM PS/2 host adapter (Model PC4) requires an additional initial step. For the PS/2 you first copy the Iomega Adapter Description File to the system reference diskette. This allows a Micro Channel bus system to recognize the Iomega host adapter when installed.

The parenthetical reference to drives above is to cover both internal and external configurations. When you install a pair of drives in the PC or PS/2 drive slots, for example, the drives are physically and electrically connected, then internally connected to the host adapter board's on-board connector. By contrast, the externally mounted Bernoulli Box drives are externally connected to the host adapter board's rear connector.

Can you use both connectors for multiple (both internal and external) drive configurations? Yes and no. I tested various possibilities. Before I tell you the results, I want to tell you that connecting more than two external or two internal Bernoulli drives to any one system is highly unusual, having little practical purpose (something reviewers like to explore). However, one practical use would be in a corporate PC environment switching from 8-inch to 5.25-inch media. A built-in compatibility with 8-inch Bernoulli drives exists, since the SCSI host adapter board used for all recent Bernoulli drives is basically the same board with a 50-pin edge connector added for internal cabling. The 37-pin external connector (on the back of the board) allows the connection of 8-inch (10- or 20-Mbyte) half-height external drives. Once connected, these drives become active as the next available DOS drive letters. This accommodates users switching to the new drives from a large library of 8-inch cartridges.

An exception to this built-in compatibility is the Bernoulli Box Plus (mentioned previously). It is not recognized by the new host adapter boards because of the slightly different interface required for its (80-Mbyte) hard disk. Coexistence of the two systems — Bernoulli II 5.25-inch systems and Bernoulli Box Plus 8-inch systems — can be accomplished by using two host adapter boards. Re-addressing one of the host interface card's port address settings by resetting switches on the board eliminates conflicts.

I could not connect either three or four 5.25-inch drives to the same host adapter. I tested this with both the AT-bus (Model PC2/50) and Micro Channel (Model PC4) host adapter boards without success. In both cases, the host adapters would recognize either the internal drives or the external drives, but no combination of both. Iomega tech support told me that using both connectors simultaneously should work, and I might have faulty host adapter boards. Since this falls in the gray area of an "unusual reviewer configuration," I didn't pursue it further.

Life is simpler in the Macintosh environment (would Mac users tolerate anything less?). First, only the external Bernoulli Box II (single or dual) is available. Second, host (adapter) interface electronics are built into the Mac Bernoulli boxes. You can connect multiple units through the Mac's SCSI port by daisy chaining them together. Since the 8-inch Bernoulli boxes are also available for the Mac, intermingling sizes on a single Mac system should be easily accomplished by daisy chaining (I did not test this). The older 5.25-inch, 5-Mbyte Mac Bernoulli Box used the Mac's external disk drive port, hence it should (not tested) also be able to coexist with the new Bernoulli Box IIs.

## Software installation and use

For PC and PS/2 systems, a setup program acts as an expert system to simplify both hardware and software installation. New Bernoulli Box users can use this excellent program and Iomega's "Quick Setup Instructions" card as a guide for the entire installation process. The menu-driven Setup gives you four options:

- Install the RCD software only.
- Install the adapter board only.
- Install the RCD software and the adapter board.
- Prepare a removable disk cartridge for use.

The nicely illustrated instruction card shows the steps involved for each of the options.

Basically, software installation on a DOS system requires copying the Iomega utility software and device driver to a directory and creating (or modifying) the config.sys file in the boot disk's root directory. Setup does both of these tasks. The config.sys file must contain a Device statement specifying the Iomega device driver (such as device=c:\iomega\rcd.sys) and a Buffers statement for a minimum of eight buffers.

The RCD device driver, rcd.sys, now has two options (Fast Host and No Verify) that can be specified with the driver. The Fast Host option helps the host adapter board perform at maximum levels in some host computers with faster clock speeds. The No Verify option turns the automatic verify function of the Iomega device driver off, allowing only the DOS Verify command to control whether or not files are verified. Normally, the Iomega device driver performs verification (regardless of the setting of the DOS Verify command) to help ensure data integrity as files copied to its Bernoulli disk cartridges are written. Both options are specified as command line switches of the Device statement in the config.sys file. /f is used for Fast Host and /nv for No Verify.

If the boot disk is a Bernoulli drive cartridge, it must first be formatted. Setup allows formatting a cartridge and transferring DOS to a new bootable cartridge. It conveniently steps through the installation of Bernoulli drive hardware and software, examining the system's configuration and recommending switch settings and other options. The factory switch settings and Setup should suffice for most users. The remaining documentation provides the information needed for custom installations.

Once the initial setup is complete, the Bernoulli drive is accessed for all operations like any other DOS disk. Just five DOS commands will not work with the Bernoulli drives: Backup, Restore, Diskcopy, Format, and Fdisk. The Bernoulli replacements come with those utilities (all have the same name, except Partition replaces Fdisk). Two additional utility commands, Install and Tools, are provided. All the utility commands (except Partition) can be executed from a command line (the DOS prompt) or from the RCD system menu.

Menu operation is fast and efficient. The Format command for the Bernoulli II drives does not require specifying an interleave factor (as was required of 8-inch-drive users to optimize performance on a particular PC system). The interleave factor is established during cartridge formatting. An interleave factor of four was used for PC-XT systems. Faster 80286 systems use an interleave factor of two. The Bernoulli II drives use an interleave factor of one.

The Install utility performs the software installation functions of the Setup program, allowing the creation of another bootable cartridge. The Tools utility allows locking and unlocking the Bernoulli drive latch pin to prevent inadvertent cartridge removal (handy for network use) and enabling or disabling the 8-inch cartridge Disksaver feature.

Like 8-inch Bernoulli drives, the 5.25-inch Bernoulli drives have a noticeable idiosyncrasy that may unnerve some users. In the 8-inch drives it's the ticking sound that occurs every second, caused by the random seek feature (called Disksaver) that keeps the head moving in a random pattern to minimize waiting time and prevent excessive wear on the media. In the 5.25-inch drives a slight, but distinct, clunk occurs after 15 to 20 seconds of inactivity. It actually sounds as though the cartridge shutter is closing, but it results from the head mechanism being parked away from the cartridge media. This prevents excessive wear on the media and extends the life of the cartridge. Impact on performance is negligible, since the recovery time from the park position is about 200 ms. It may take a little while to get comfortable with this new sound.

For Macintosh (Plus, SE, and II) systems, you start by inserting the Iomega Utilities disk. Then load the SCSI device driver by pressing the Command and Option keys while double-clicking on the driver icon. After the driver has been loaded, you can insert a new Bernoulli disk cartridge for initialization. A dialog box will ask if the disk should be initialized. When you respond affirmatively, the cartridge will be initialized, taking about 15 minutes. A cartridge name dialog box allows you to assign a name. Initialized Bernoulli cartridges appear using a distinct icon on the Finder desktop. Next, copy the System Folder from the Startup disk to the cartridge. Repeat these steps to prepare other cartridges for use.

You can start the system from the Bernoulli cartridge by removing any floppy diskettes and executing a restart. If you start the Mac from a floppy or hard disk, the Iomega SCSI device driver must reside in the System Folder of the Startup disk. For compatibility with the Iomega driver, the System Folder must contain System version 4.2 and Finder version 6.0 or newer. When the driver is in the Startup disk's System Folder, the Bernoulli Box will be recognized at startup time; hence, you will not have to manually load the driver.

In addition to the SCSI driver, the Utilities diskette contains the Iomega Workshop. Workshop contains the programs necessary to format and back up Bernoulli cartridges, set Bernoulli Box options, and run diagnostic tests. A Megacopy utility provides "intelligent" backup. Megacopy gives you the flexibility to select files for backup by disk, name, date, application, or those modified or created since the last backup. You can back up hard disks to cartridges, cartridges in a single-drive system, and cartridges to diskettes.

The Workshop operates like most Mac application software. You start it by either double-clicking its icon or selecting its icon and then Open from the File menu. Only the Bernoulli cartridge icons will appear in the Workshop window. These icons are manipulated (selected, dragged, and ejected) using the same methods you use on the Finder desktop.

The Workshop menu bar shows File, Edit, Option, and Special selections.

The File menu selections are Get Info, Megacopy, Print List, Eject, and Quit.

The Option menu offers two choices — Verify Writes and Auto Flag — that affect only a selected cartridge, but protect data integrity and performance. Enabled upon formatting of the cartridge, they are changeable only if the cartridge is not write protected. Verify Writes helps insure data integrity by verifying all files written to a cartridge as they are written. Auto Flags allows a Bernoulli drive to automatically replace bad sectors with spare sectors as files are written on a cartridge.

The Special menu provides the two diagnostics Surface Scan and Drive Test, and a Write Driver and Erase Disk utility. A Surface Scan Results window displays the results of the analysis, and a hard copy can be obtained using the Print Lists (File menu) command. The Erase Disk utility allows erasure with (long format) or without (short format) a cartridge surface verify, and a special A/UX option can be used to format a cartridge in the Apple Unix (A/UX) format.

## File exchange — PC or PS/2 and Mac

The Bernoulli File Exchange is an optional ($149) software package for Mac users. It opens up an effective bridge for transferring data between PC and PS/2 systems and the Mac. The Bernoulli File Exchange allows two-way data sharing. It allows the Bernoulli cartridge systems to become file sharing devices. Data on DOS formatted cartridges appear as standard file folders and data files on the desktop of a Mac. Further, the data on a Mac formatted cartridge appears in standard DOS format on a PC or PS/2.

The Bernoulli File Exchange device driver resides only on the Mac. You install it by simply dragging the Bernoulli File Exchange device driver icon to the System Folder of the Mac Startup disk. The driver is loaded into memory during startup and a welcome (logo) screen showing the version number is displayed. After startup, a DOS cartridge inserted into the Mac's Bernoulli Box will appear as a Bernoulli cartridge icon on the Mac desktop. The driver makes the DOS cartridge act like a Mac cartridge. When its icon is opened, its contents are displayed like Mac folders and documents. The names of the folders and documents exactly match the DOS directory and file names. The documents (DOS files) can be opened and edited by an appropriate application program. When the two environments (Mac and DOS) share a common file format (such as ASCII or Pagemaker files), the Mac will have full use of the data.

My first test of the Bernoulli File Exchange was under fire (sort of). I used electronic mail to transfer an ASCII delimited text file, developed with a DOS word processor, to a Mac user. He sent me back a message saying that there appeared to be unwanted characters in the text file at about 80-character intervals when he read the file into Microsoft Word (Mac version). He wondered if I could clean it up so he didn't have to edit every line. I took another look at the file using Word (DOS version) and saw no such problem; the text was contiguous. Before I sent him a message questioning his sanity, I thought I had better view it using the Mac version of Word. To do this, I simply copied the file to a DOS-formatted Bernoulli cartridge, inserted the cartridge in the Mac Bernoulli Box, and opened the file from Word. Sure enough, his complaint was valid.

Since the file was short, and I was the original author, I corrected it using the brute-force technique; I edited the file with Word. Then I brought the cartridge back to the DOS system and transferred the edited file back to him. The bridge the Bernoulli File Exchange establishes is very effective and the steps are actually format transparent. I never had to concern myself with the format of the file.

## File exchange — PC and PS/2

Another handy application of file exchange I found for the Bernoulli systems was in a DOS environment, but between a PC and PS/2 — a Compaq Deskpro 386 and an IBM PS/2 Model 80-111. Pre-Bernoulli, the Compaq had just one 5.25-inch, 1.2-Mbyte floppy drive and the PS/2 had just one 3.5-inch, 1.44-Mbyte floppy drive. File exchange between the two machines was accomplished using Traveling Software's excellent Desklink/Laplink programs connected with twisted-pair phone line. Certainly there is nothing wrong with this type of solution. It's just not the same as having direct access to the files on interchangeable cartridges.

**Table 2. Retail prices for 5.25-inch systems.**

| | |
|---|---|
| Single Drive 44-Mbyte External Subsystem | $1,799 |
| Dual Drive 44-Mbyte External Subsystem | $2,799 |
| 44 Mbyte Internal Master Drive Kit | $1,399 |
| 44 Mbyte Internal Slave Drive Kit | $1,099 |
| Single Drive 20-Mbyte External Subsystem | $1,450 |
| Dual Drive 20-Mbyte External Subsystem | $2,350 |
| 20-Mbyte Internal Master Drive Kit | $1,100 |
| 20-Mbyte Internal Slave Drive Kit | $900 |
| Single Drive 44-Mbyte External Subsystem (Mac) | $1,799 |
| Dual Drive 44-Mbyte External Subsystem (Mac) | $2,799 |
| Single Drive 20-Mbyte External Subsystem (Mac) | $1,299 |
| Dual Drive 20-Mbyte External Subsystem (Mac) | $2,299 |
| Host Adapter and Software — PS/2 | $399 |
| Host Adapter and Software — PS/2, Bootable | $399 |
| Host Adapter and Software — PC | $200 |
| Host Adapter and Software — PC, Bootable | $280 |
| Bernoulli File Exchange Software (Mac) | $149 |
| Tri-Pak, 44-Mbyte Disk Cartridges | $375 |
| Tri-Pak, 20-Mbyte Disk Cartridges | $249 |

Installing a Bernoulli system on each machine creates an ideal file-exchange environment. The cartridges are completely compatible across the two machines, so file exchange becomes as simple as swapping the large capacity (21- or 44-Mbyte), high-speed Bernoulli cartridge disks between the two machines. Ideally, the Bernoulli drives on the two machines will be set up for identical drive letters.

The best part of this scenario is the Bernoulli cartridge's primary storage feature. Bernoulli cartridges are primary storage systems, with the contents always fully executable. This means that when a single Bernoulli drive is used on an existing hard disk system, the cartridge can be used as executable or "working" backup for the hard disk. Unlike archival tape backup systems that can only store the data for subsequent recovery, a working backup cartridge offers the advantage of full operation in the event the system's hard disk crashes. This takes on new meaning in the file exchange scenario. It provides executable access to entire application directory structures, allowing application exchange between the two machines.

This application exchange means that large, complex application structures can be swapped between PC and PS/2 systems equipped with Bernoullis. I found this particularly handy for desktop publishing, databases, and computer-aided systems/software engineering (CASE). Of course, the costs associated with this kind of setup will be a lot higher than other solutions. But think of the potential to improve productivity. In many situations this could easily justify the additional expense. I only wish this capability existed for the OS/2 operating system. Iomega has not yet released an OS/2 device driver for the Bernoulli systems.

**Summing up.** I've always held a high opinion of Iomega's Bernoulli systems. After this comprehensive evaluation period my opinion is even higher. In all, I configured and tested a total of seven Bernoulli drives on three different computers ... without a single failure. The only operational problem I encountered was when I stretched the limits of practical coexistence, attempting to connect internal and external drives on the same host adapter.

Compared to the 8-inch Bernoulli systems, these new 5.25-inch Bernoulli II systems are superior products. It's not just the cartridge size, either. The Bernoulli IIs are much quieter. The external boxes are much smaller and more manageable. The drive operation is even simpler, using only pushbuttons instead of both pushbuttons and levers. Of course, quieter is relative. You are actually adding noise when you connect a Bernoulli Box to a (fanless) Mac. But you shouldn't have a problem living with it, especially if you don't have a hard disk connected. Once you try the handy-sized 5.25-inch Bernoulli II systems, you'll find it awfully hard to return to the larger 8-inch systems.

Bernoulli systems have always cost more than similar-capacity hard disks, but their unique performance, reliability, and versatility still rank them as a preferred mass storage alternative. When you require one or more of their unique features, they're awfully hard to beat.

See Table 2 for a list of 5.25-inch system prices. Contact Iomega Corp. at 1821 West 4000, South Roy, UT 84067, phone (801) 778-3000. — *G. Perrone*

**Reader Service 21**

# Optimized protection and superior reliability

At almost any computer show you can find several vendors hawking uninterruptible power supplies. These devices have the graceful design and seeming usefulness of a breadbox that takes up more room than the average computer. As a result, I never would have thought I wanted or could use a UPS. But, having used the Proxima U5 (also called the IPS, or Intelligent Power Supplies, 500+) from Computer Accessories for several weeks now, I am a changed person.

When I first was asked to review the U5, I was hesitant. Only mildly interested in what they had to offer, I envisioned a device that occasionally would rescue me when the public utility decided to pull the plug before I had saved the monumental changes I had just made to an important document. But, since I use a word processor that automatically and regularly saves my most recent modifications, I didn't really think I needed a UPS.

However, when the U5 arrived, it was not at all what I expected. On first glance I thought I had been sent the wrong unit. What I received looked more like a power director to replace a perfectly good and inexpensive power strip I had used for years. The unit measures a modest 14 × 14.8 × 2.4 inches high.

Picking the unit up and finding it surprisingly heavy (23 pounds), I soon realized that this was no ordinary power director. Hidden inside the streamlined case was a sealed 4-amp-hour lead-acid battery and an inverter. Indeed, closer inspection revealed the power saver section (complete with battery-ready and reserve-time front panel lights) that provides the interruptible power.

## An intelligent design

One of the key elements in the design of the U5 was the Motorola 6805. Using a microprocessor reduces the component count by 35 percent, thus both reducing heat (this device does not include a fan) and the number of components that can fail. More importantly, a microprocessor makes the system "intelligent" — the device includes digital control and a number of self-test assurance checks. For example, when first turned on, the U5 switches to emergency power and runs your system off the battery. For anyone who has learned from bitter experience that you constantly need to check that your backup works, this form of self-test is clearly very intelligent.

After checking to make sure the battery is okay, the unit switches to line power. The audible alarm beeps to tell you both the status of the battery (fully charged or requiring charge) and to indicate if an internal fault or an overload exists. The overload occurs when too much equipment is plugged into the three emergency power outlets. In addition to the audible alarm, an overload light comes on. An internal fault requires factory service.

Normally, no faults are indicated, and the battery-ready light will come on as soon as the battery returns to full power. So, you use the power director portion of the unit to activate whatever devices you want to start using. In my case, I have the CPU and monitor, as well as my external modem, plugged into one of the UPS outlets. (The box fits conveniently between your computer and your display.) I don't really expect to need emergency power for the modem, but what the heck, it's nice to know I won't be dropped immediately when logged on to some external system and the power fails. Also, the system allows me to turn the modem off when I don't need it.

The two auxiliary switches now control my two line printers, which I find particularly handy. Before, I was always wheeling my chair over to one or the other of them while trying to find the elusive on/off switch.

The real test for me was how long the U5 would continue to run when the plug was pulled. Since I have a fully loaded 386 system with every slot filled, I wasn't expecting too much time. It came as a surprise when the U5 was still chugging away after nearly 20 minutes. True, I was only supplying the CPU and monitor, but I don't expect to have to power a line printer under emergency conditions (although this unit could). But, if you need all the power you can get, you can plug in an optional external battery pack to nearly triple your backup time.

**Computer Accessories' Proxima U5 (IPS 500+) combines all the features you could want in a sleek cabinet that fits between your computer and your display.**

You might ask, how do you know when the U5 switches to battery power? The answer is, the reserve lights come on and you hear a buzzing sound. Shortly thereafter you hear the audible alarm, which you can turn off by pressing the alarm defeat button. Returning to line power causes the lights to go off and the battery-ready indicator to remain off until the batteries are recharged. For me, recharge time was measured in minutes, but a fully depleted battery will take up to eight hours to recharge.

If this were all the U5 had to offer, it would be well worth its rather modest price of $750. But there is really a lot to this unit. Besides being a UPS with switches, the U5 includes protection against RFI/EMI noise, over- and undervoltage conditions, and spike/surge suppression. Also included is a pair of phone jacks for phone line conditioning for your modem. The Proxima nameplate cleverly serves as an antistatic touchplate, as well. And, for the consummate LAN user, the network interface jack in the back communicates through an auxiliary optional interface assembly to either a Novell or 3Com server to automatically save data and shut down an unattended network after a power loss.

**Summing it all up.** I have demonstrated this U5 to a number of visitors, and each was immediately impressed both by its sleek design and impressive list of features. But the real test came each time I pulled out the plug and my computer just kept on chugging. Except for the slight buzzing sound and some monitor EMI (fast-moving scan lines scrolled up the screen), you wouldn't have realized that the line power had disappeared. After power was restored, everything went back to normal. One exception, however, occurred on a particularly hot and muggy day when the power company was running at the lower edge of an acceptable voltage level. Then the U5 decided it was better to use batteries for a while.

The only drawback I noticed was that the telco jacks only protected two of the four wires that passed through it. So, if you use a two-line RJ11-style cord, you won't have full protection.

On balance, the U5 provides an excellent example of intelligent packaging and microcomputer utilization. It combines all the features you could want in a handsome, low-profile UPS/power director. I rate it outstanding in its class.

Computer Accessories Corp. is located at 6610 Nancy Ridge Dr., San Diego, CA 92121, phone (619) 457-5500 or (800) 582-2580. — *R. Maulucci*

**Reader Service 22**

# hDC Windows Manager

When it comes to producing exciting and fun software releases, hDC Computer Corp. rates number one in my book. Over several issues we (Noah Davids and I) have looked at and raved about their first two releases, hDC Windows Express and hDC Windows Color. Now comes hDC Windows Manager, and it, too, is a winner.

Those of you who use and enjoy Microsoft Windows probably have recognized the need for some add-in software to make the basic release more palatable. Windows Express from hDC replaces the MS-DOS Executive Window, making it easier and more natural to activate programs. Windows Color adds the missing colors to the basic environment. Now, Windows Manager brings the convenience of pop-up utilities to expand on the features Windows offers.

The idea behind Windows Manager is one of expanding and customizing your Microsoft Windows system. This translates into an expansion of the normal Windows control menu to include a second column of Windows Manager applications. This second column can be either part of every window or a separate Windows Manager icon that you can activate and expand as needed. If part of every window, then the little oval (the icon for the control-menu box) at the top of every Windows app is replaced with an hDC icon to indicate the second column's availability. As MicroApps are added and removed, the list of options in the second column expands and contracts. This feature supports future additions to the basic MicroApps set that comes with the current release.

Interestingly, Windows Manager is so well integrated into Windows that you would be hard pressed to remember that it's an add-on piece of software rather than part of the original release. This seamless integration of hDC software makes you wonder how they do it and do it so well.

## Installing and learning to use Windows Manager

Installing Windows Manager is painless. After starting up Windows, you merely run the Install program from the MS-DOS Executive Window. You are asked a few questions, which most likely you will simply acknowledge, and the software is copied to your hard disk. The installation process modifies the win.ini file as necessary and even checks to make sure your hDC library is current (if not, it replaces it with the latest distribution). After that you are free to experiment with Windows Manager to become familiar with it.

The manual starts off in tutorial mode, letting you explore the basic functionality of Windows Manager. Concluding chapters cover the MicroApps in depth, tips and techniques, Q & A, and a glossary. Lots of screen shots, a table of contents, and an index round out this short but well done manual. In addition, all screens include context-sensitive on-line help.

## The MicroApps

Windows Manager consists of seven MicroApps, including an alarm clock, an auto save feature, customization of the desktop, a font viewer, a memory-in-use display, a system enhancer, and a start-up for a selected set of applications.

The alarm clock displays the date and time and reminds you of up to three pending appointments or regularly scheduled appointments. Alarms can be silent or beep, and you can be prompted with a short note about the appointment. An auto save automatically executes the Save command of a current Windows application. (Note that this will not work for a non-Windows application, such as a standard word processor.) You can choose to have the Save operation enabled by a set number of keystrokes or minutes.

The desktop MicroApp allows you to dress up your start-up screen and the background pattern, and enable a customized screen saver. One option for both the start-up screen and the background allows you to import bitmaps generated by a paint program. For start-up you can select an effect, such as zoom, pan, coalesce, or fade, while for background you can choose the foreground color and whether you want a single or a repeated image. The screen save offers two options besides the bitmap — random polygons or rocks — whenever screen activity is dormant for a specified amount of time.

The font-viewer MicroApp is the simplest of the bunch and also one of the most valuable. It presents a scrollable display of either the screen or printer fonts installed under Windows. In much the same way, the memory viewer offers vital information — how the base and extended memory are being used — through the simplicity of either a pie or bar chart. Even in icon form, the memory viewer will continue to show the amount of base memory free. My one complaint here is that, on a 386, the amount of base memory is not the total amount but the amount after Windows has taken a bite for the swap area. Thus, the total will be more like 384 Kbytes rather than 640 Kbytes on a fully populated base memory.

The system enhancer is a general-purpose MicroApp for running programs, arranging windows (overlapped, tiled, or as icons), closing all Windows apps (but not non-Windows apps), and ending the Windows session. In some ways this overlaps the earlier hDC product Windows Express, but it actually offers more versatility.

Finally, I found Work Sets interesting. Using this MicroApp means that you can initiate different sets of Windows programs, as well as save the current state of any Windows session for later recall. It is equivalent to dynamically managing the win.ini file to decide what should be started up either upon entry to Windows or later, when you need to initiate a set of applications.

**Summing up.** While you may not need or use all of the MicroApps that come with hDC's Windows Manager, you certainly will enjoy trying each one out to decide what's best for your application. For example, I tried the desktop and enjoyed the customization of the various screens it offered. But, in the long run, I decided not to use the desktop because it wasn't as valuable to me as the font and memory viewers. These two MicroApps are so informative and helpful that I set my system so they come up whenever I start Windows.

The idea of Work Sets was very appealing and resulted in my putting together sets of applications that I can now call up whenever I switch from one task to another. Specifically, it lets me put together a command window and a text editor window whenever I bring up my communications program in another window. Alternatively, it brings up a command window and my cardfile window whenever I bring up my word processor.

As a $79.95 utility, Windows Manager is both reasonably priced and quite valuable. I run it on a 4-Mbyte 386/20 with Windows version 2.11 along with Windows Express, and I have lots of memory left to run other programs. I enjoy both the added flexibility and increased Windows utility it offers. Thus, Windows Manager ranks as another hit for me, and I heartily recommend it.

Contact hDC Computer Corp. at 15379 NE 90th St. Redmond, WA 98052, phone (206) 885-5550. — *R. Eckhouse*

**Reader Service 23**

# Portability at a price

I won't try to defend the price you pay for a Toshiba 5200, but I will tell you it's the Cadillac of portable computers. It's clearly more than a laptop. It weighs too much, nearly 19 pounds, and it's pretty bulky, measuring 14.6 × 3.9 × 15.6 inches. But when you realize that you have a 20-MHz 386 with a 100-Mbyte disk drive in an easily transported package, you recognize the T5200 as the ultimate in portable machines.

In my environment I often need to set up a machine on top of someone's desk in a hurry. It's a real pain to do so when you're talking about a desktop machine with its separate components and nest of dangling cables. The T5200 is extremely simple to transport, in most cases requiring only that you remove the power plug and close the case.

Speaking of power, this machine does not operate from a battery. However, it does have an auto-sensing, universal power supply, which means that with the right plug you can use this machine anywhere you can find 90-250 volt, 50-60 Hz AC power.

**Toshiba's T5200 combines a 20-MHz 80386 with a hard drive to provide a portable powerhouse.**

Besides having a 386 and either a 40- or 100-Mbyte hard drive in the cabinet, the T5200 has 2 Mbytes of memory (internally expandable to 8 Mbytes total) using a 32-bit data path to system memory and a 32-Kbyte static RAM cache, a 3.5-inch 1.44-Mbyte floppy disk drive, a VGA plasma display, two serial ports, and a multiple-use parallel port. When I say multiple-use parallel port, I mean that it can serve as a standard printer, a bidirectional parallel, or an optional external floppy port.

Also, carrying on the tradition of the T3100, you get two expansion slots, one for an 8-bit half-length IBM PC-compatible card and the other for a 16-bit full-length card. The 8-bit slot has dual edge connectors so you can use either a standard PC or a special Toshiba card, such as for a Toshiba modem.

As I mentioned, you can expand the memory from the base of 2 Mbytes to 8 Mbytes using Toshiba's proprietary optional 2-Mbyte memory modules, priced at $999 each. You don't need an expansion slot because the modules fit into connectors on the memory board. Inserting modules on the memory board requires some disassembly (the board is located under the keyboard), but the reference manual thoroughly documents the procedure.

Other options include a 2,400 bps Hayes-compatible modem, an external 5.25-inch floppy drive, an expansion chassis with five IBM PC-compatible slots, and either a leather or fabric carrying case. One option not available is an external keyboard.

The model with the 100-Mbyte hard disk has a 25-ms average access time, while the 40-Mbyte model has a hard disk with an average access time of 29 ms. Those who go with the 40-Mbyte drive can later upgrade the hard disk to a 100-Mbyte drive.

As in most laptops, everything is compactly arranged in the standard clamshell case, yet very accessible from either side or the back. The left side provides access to all the expansion boards. At the back are the serial, parallel, and RGB ports, along with the on/off switch and power cable. Along the right side you'll find the 3.5-inch floppy drive. A quiet but audible built-in fan keeps the unit cool during operation.

The keyboard on this machine is a cross between the enhanced 101-key type found on most AT-class machines and the original PC keyboard. The 91 keys include a separate keypad and 12 function keys. Adjacent to the space bar on both sides are Ctrl and Alt keys. The escape key is at the top left. The Caps, Num, and Scroll Lock lights are well above the keyboard, just under the plasma display on the right, and the power, hard disk, and floppy disk in-use lights are to the left. Also on the right side is a security bracket, if you want to tie down this expensive machine while you're on a trip. In fact, the cover includes an integral combination lock just like you'd find on a briefcase.

The plasma display is VGA compatible, with a resolution of 640 × 480. Visibility is excellent in all kinds of lighting. A brightness control, although available, has a limited range.

The font set for this display is both clumsy and poorly defined for characters with slanted strokes (for example, the A and the V). When switching the cursor from insert to overtype modes in my word processor, the shape changed from three lines at the top to a single line at the bottom. On all other machines I've tested, it normally changes from a half block to an underline. While Toshiba may have made it possible to change this, the manuals did not tell me how.

As with any plasma display, I found it difficult to make out the various shades of gray representing color. However, the Toshiba folks have thoughtfully provided an RGB connector at the rear, making it extremely easy to connect up an analog monitor for those times when you need color. In fact, if you want to, you can remove the plasma display completely and keep only the base unit, without cover, on your desk.

Like other Toshiba machines I've looked at, the T5200 comes with an excellent set of manuals, complete with b/w as well as color figures and pictures of the system components. The manuals include one called "The First Time," which quickly gets you up and running; a thorough reference manual; and a MS-DOS

3.3 Operating System manual. Each has a table of contents and a good index. Toshiba has also provided a floppy-based hypertext help system for those times when you need help but don't want to carry the manual set with you. The hypertext help includes separate modules for operating the T5200 and using MS-DOS.

In addition to MS-DOS (but not Basic), you get a setup, configure, self-test utility; QEMM-386 version 4.20; and PC-Kwik Power Pak. Add your own software and you're up and running.

I can't say much more about the machine technically. It performed flawlessly during the period that I evaluated it. It also drew a number of people over to look at it and remark that they wished they had one. As I've said, it's everything you could want in a machine, is Windows compatible, and is claimed to be OS/2 compatible as well. It runs every piece of software I could think of, works with my Logitech serial mouse, and accepted my Artisoft LANtastic network card without a hitch. Let me add that having the LAN card in the machine made it an instant performer, since I could rapidly move files back and forth between machines on the LAN and could remotely print files without tying the T5200 down to a printer.

I rate this machine excellent but a bit expensive ($8,299 for the system with the 100-Mbyte drive and $7,699 with the 40-Mbyte drive). However, many mail-order houses discount the machine a fair bit, so in the end you won't pay that much more for this portable than for a desktop machine. Also, you do get a one-year exceptional care warranty that provides a loaner sent overnight once you have returned your T5200 for repair.

During the course of this review, the highly utilitarian T5200 fit into an environment where we often need to place a sophisticated computer on someone's desk for only a short period of time. For that reason I have chosen to buy the machine for my permanent use. Need I say more?

Contact Toshiba America Information Systems, Computer Systems Division, 9740 Irvine Blvd., Irvine, CA 92718, phone (800) 457-7777. — *R. Eckhouse*

**Reader Service 24**

## Product notes

**File transfer.** When it comes to file transfer programs, I find all that I've tested to be useful and effective. Little distinguishes one from another except for the extra features to differentiate its product. After all, when it comes to the basic transfer mechanism, none can really exceed the speed of either the parallel or serial port, or the speed of the underlying CPU chip (8088 at 4.77 MHz or better). Thus, the smart shopper will make the buy decision based on price (Are the necessary cables included?), availability (Who plans ahead?), and extras (Do you want to perform more than simple file transfers?).

File Shuttle version 4.1 from GetC Software, 1280 Seymour St., Vancouver, BC V6B 3N9, Canada, phone (604) 684-3230 or Box 8110-182, 264 H St., Blain, WA 98230-8110, USA, is a capable, easy-to-use file transfer program with a couple of nice twists.

First, it includes the "Rocket Socket," a Centronics-to-D-25P converter plug. Since nearly every machine has a printer attached, this plug makes it easy to disconnect the printer cable at the printer end (remember, it's held on not by screws but by clips) and connect the printer cable to your laptop or second machine to transfer files via the parallel port (the faster of the two options, serial/parallel). Thus, when you travel you do not need to carry along a set of cables but can slip this small connector into your pocket instead. Of course, File Shuttle also works with serially connected machines, but needs a cable.

Second, the software operates intuitively, so the manual can be direct and blessedly brief. While this may not appeal to novices, it means that you can skip the manual and use the context-sensitive help screens instead. If that doesn't work, a "Menu Functions and Key Definitions" chart explains all the information you are likely to need to use this program

Third, you use the same software on both machines, so you don't have to remember to run a master program on one and a slave on the other. As a consequence, you can control the sending and receiving from either machine. And, since you can take the program out of auto mode, it means you have an extra level of control so you don't send in the wrong direction and wipe out the files you are trying to move.

Last, command features allow you to enter a DOS command or run a program, execute File Shuttle in command line mode rather than as a menu-driven program, and record, trace, or execute macros commands.

File Shuttle comes on both 5.25- and 3.5-inch floppies; can operate in English, French, German, or "Shuttle" modes; and allows you to select what to transfer from either a file or directory tree list. Thus you can quickly mirror-image one hard disk drive to another or pick selected subtrees. Send options allow you to pick files that have the archive bit set and update the bit after transfer, to select hidden files, and to select files either using wild cards or by date. Also, transferred files can be sorted by name, extension, date, and size. No question about it, this $119.95 program has a lot going for it. I liked it, I will continue to use it, and I recommend it to you. — *R. Eckhouse*

The **Tandy 5000 MC** offers both Micro Channel architecture and IBM Model 80 compatibility. The high-speed data transmission of Micro Channel architecture is complemented by the high-speed processing of the Intel 80386 microprocessor. Features of the machine include:

- IBM Model 80 compatibility, using MS OS/2, MS-DOS, or Xenix versions of PS/2 system software;
- five IBM Micro Channel compatible slots (two 32-bit and three 16-bit slots);
- an on-board VGA with 16-bit upgrade slot;
- a 20-MHz 80386 CPU;
- 32 Kbytes of cache memory;
- a removable CPU board;
- 2 Mbytes of memory standard, upgradeable to 16 Mbytes;
- a reference diskette with advanced software, which automatically configures the system;
- a high-capacity, 1.44-Mbyte, 3.5-inch disk drive;
- four drive slots (for two internal floppy disk drives and two internal hard drives, 3.5- or 5.25-inch);
- a real-time CMOS RAM clock;
- mouse, serial, and parallel ports;
- a socket for an optional math coprocessor (Intel 80387-20); and
- a 101-key enhanced keyboard.

The Tandy 5000 MC comes with either a 40- or 80-Mbyte hard disk drive installed and low-level formatted (a utility to reformat the hard disk is included on the reference diskette). Access times for the 40- and 80-Mbyte drives are 19 and 16 ms, respectively. The drive controller is a standard ST-506 using MFM recording.

The VGM 200/300 is a high resolution, noninterlaced, 14-inch color monitor with picture controls for brightness and contrast. Resolution modes include 720 × 350, 720 × 400, and 640 × 480. The VGM 300 Monitor costs $629, and the Tandy 5000 MC is $9,491.90. Both are produced by Radio Shack, a division of Tandy Corp., Fort Worth, TX 76102, phone (817) 390-3300. — *M. Dediu*

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# NEW PRODUCTS

Contact or send releases to Nancy Hays, *Computer*, 10662 Los Vaqueros Circle, Los Alamitos, CA 90720; Compmail+, n.hays

## Accel redesigns Tango-Schematic for Series II release

Accel Technologies has redesigned its Tango-Schematic for release as Tango-Schematic Series II. According to the company, this menu-driven schematic-capture software allows designers to draw schematics on screen, create new library components, perform a design rule check, generate netlists, and produce schematic drawings.

The software's component libraries contain more than 5,000 parts customized by Standard Engineering Data Company (Sedco). Each component comes in the standard commercial symbolic representation and the ANSI/IEEE Standard 91-1984 symbolic representation, according to Accel.

Technologies covered in the libraries include TTL, CMOS, ECL, microprocessors and peripherals, PLDs, linear ICs, transistors, diodes, connectors, electromechanical parts, and passive components.

Tango-Schematic supports hierarchical or flat schematic designs with up to 99 sheets per level of hierarchy. It also supports both homogeneous and heterogeneous components.

User documentation includes a 400-page manual with tutorial, reference, command summary, examples, and index. On-line help includes more than 100 screens of information with index.

The program generates files in DXF and Postscript format and works with most printers and plotters, according to the company. Tango-Schematic supports ANSI A-E and ISO A4-A0 size drawings and scales drawings to any sheet size.

Reports generated include Bill of Materials, Part Usage, Design Statistics, Hierarchy Tree, Cross Reference, Library Contents, and Part Location. Post-processing includes netlist generation, design rule checking, forward annotation, back annotation, generation of a library archive for the design, and schematic cleanup.

All operations are reportedly accessed from a single integrated program. Users can exit temporarily with the Suspend to DOS function.

Tango-Schematic Series II runs on IBM PC, XT, AT, PS/2, and 386 PCs and compatibles. It costs $495.

**Reader Service 30**

## Mechanica assists design engineers

Rasna's Mechanica family of design analysis tools targets mechanical design engineers. According to the company, the tools allow design engineers to evaluate and refine designs.

Applied Structure, a structural design analysis tool, incorporates the company's proprietary Geometric Element Analysis, which eliminates finite element meshing. The software reportedly provides automatic adaptivity, meaning the user specifies solutions' level of accuracy.

Applied Structure also offers automated sensitivity analysis and design optimization.

Applied Structure is scheduled for the first quarter of 1990. It will cost $9,000.

Applied Motion, a mechanism design analysis tool, uses the company's Rapid Mechanism Modeling for model preparation. Users enter geometric shapes to define models. Equations are internally translated into problem-specific C subroutines. They are then compiled, linked, and executed.

The software also includes a sensitivity analysis feature and error diagnostics.

Applied Motion is scheduled for the second quarter of 1990, at a price of $9,000.

The initial releases will be integrated with AutoCAD and compatible with Sun Microsystems Unix workstations and DOS-based 386 PCs.

**Reader Service 31**

## Gould library provides soft megacells

Gould AMI has announced a library of soft megacells, which are configurable standard cells. These standard cells consist of logic gates for performing board-level functions, according to the company. They can be merged onto a single chip, along with the necessary glue logic.

The MG82C54 programmable interval timer is the first megacell in the family. Compatible with the 8254, it provides 20-MHz operation and three independently programmable 16-bit counters, plus six programmable counter modes.

According to Gould, a typical standard cell device including an MG82C54 and approximately 3,000 logic gates costs $4.75 each.

Other megacells under development in the MG series include the MG80C85 microprocessor and the MG82C59 programmable interrupt controller, planned for the end of the year.

**Reader Service 32**

## ACNAP lets Macintosh users analyze linear circuits

BV Engineering's AC Network Analysis Program for the Macintosh is, according to the company, a general-purpose circuit simulation program that analyzes linear circuits containing up to 200 active and passive components. ACNAP reportedly allows immediate graphing and printing of analyses and scrolling of results.

The program performs Bode, Monte Carlo, sensitivity, noise equivalent bandwidth, component iteration, spectra, and worst-case analyses. Users can create macros of unlimited length with optionally embedded comments, delays, and pauses.

Users can also create, combine, edit, and save component models and circuits to a component library as individual devices.

ACNAP requires 512 Kbytes of memory and runs on a floppy- or hard-disk-based Macintosh 512K, Mac Plus, Mac II, or Mac SE under System 3.2 or later and Finder 5.3 or later. The software supports the Imagewriter dot matrix and Laserwriter laser printers. An optional plotter driver module costs $95.

ACNAP Version 3.6 is not copy protected. It costs $349.95.

**Reader Service 33**

## Poqet PC weighs in at one pound

**Poqet's PC is an MS-DOS portable computer that runs for up to 100 hours on standard AA-size alkaline batteries.**

Poqet Computer has announced the Poqet PC, a one-pound, IBM-compatible, DOS portable powered by two AA-size batteries. Based on the 80C88 microprocessor, the portable includes 512 Kbytes of system RAM, 640 Kbytes of ROM, and two slots for RAM or ROM memory cards.

System ROM contains MS-DOS, GW Basic, BIOS, and five Poqet Tools applications. The applications include a calculator, memo and note-taking facility, scheduler, electronic card file, and terminal emulator. Another application, Poqet Link software, is an MS-DOS file manager and file transfer program that uses Virtual Network Architecture.

The display features a nonbacklit LCD screen with 640 × 200 pixel resolution and measures 80 characters × 25 lines. It supports CGA and MDA modes.

The keyboard offers all functions of a PC-AT enhanced keyboard, according to the company. It contains 12 function keys, an embedded numeric keypad, and 77 keys in typewriter-style layout.

The communications cable provided with the PC provides connections to RS-232-C serial ports. A parallel interface cable will allow connection to printers, while a serial modem cable will permit communications via phone lines.

Additional applications software will be available on credit-card-sized disks, called Poqet Memory Cards, that fit into two slots in the portable. According to the company, many of these applications are ROM-executable, thus using a small part of system RAM.

The Poqet Floppy provides additional memory space in the form of a 3.5-inch, 1.44-Mbyte floppy disk drive that operates on four AA-size batteries.

The Poqet PC costs $1,995.

**Reader Service 34**

## Apple adds portability and power to Mac family with Macintosh Portable and Macintosh IICI

Apple Computer has announced the Macintosh Portable and Macintosh IICI computers.

The new portable uses active matrix LCD technology in a display measuring 640 × 400 pixels. The system also features a video output port. Used with an adpater, it can drive external monitors, projection video systems, or overhead viewplates.

The Mac Portable includes a Motorola 68000 processor, 1 Mbyte of static RAM, lead acid batteries, a separate power-management microprocessor, integrated trackball, full-size keyboard, optional mouse (comes with the system), expansion connectors for additional RAM and ROM, 1.4-Mbyte Superdrive floppy disk drive, optional 40-Mbyte hard disk drive, connector for an internal modem, stereo sound capability, and seven external ports.

The portable uses Macintosh System software version 6.0.4 and is compatible with other Mac software.

The Mac Portable weighs 13.7 pounds; 15.7 pounds with hard disk drive. With 1 Mbyte of RAM it costs $5,799. Adding a 40-Mbyte hard disk drive takes the price to $6,499.

The Macintosh IICI is, according to the company, its most powerful Mac. The IICI incorporates a 25-MHz Motorola 68030 processor and 68882 coprocessor, burst-mode RAM access, 80-ns DRAM, a RAM cache connector, built-in video capability, 512 Kbytes of ROM, and IICX design, including three NuBus slots, 1-8 Mbytes, an internal Superdrive, and an internal 3.5-inch hard disk drive.

The Mac IICI comes with a mouse, System software 6.0.4, Hypercard 1.2.5, and documentation.

The Macintosh IICI with 1 Mbyte of RAM costs $6,269. Adding a 40-Mbyte hard disk drive takes the price to $6,969. The price for a system with 4 Mbytes of RAM and an 80-Mbyte hard disk drive is $8,669. Adding A/UX makes it $9,152.

Portable: **Reader Service 35**
Mac IICI: **Reader Service 36**

## Harris extends secure environment

Harris Computer Systems Division has extended its secure environment for the Night Hawk real-time multiprocessing computers with its introduction of the Harris SX Secure Computing Environment, which features the LAN/SX secure local-area network and 630/SX secure windowing system.

LAN/SX is offered through an agreement between Harris and Verdix, while 630/SX is offered through a joint-development agreement between Harris and AT&T Federal Systems.

The network security center hardware and software for LAN/SX cost $24,500. Individual encryption controllers cost $4,500. LAN/SX will ship in the third quarter of 1990.

The 630/SX software costs $2,500. Each terminal, including a monochrome display, 1 Mbyte of memory expandable to 2.5 Mbytes, and RS-232 connection, costs $52,000. The 630/SX is available now.

**Reader Service 37**

## Intel claims first superscalar microprocessor

Intel claims that its 32-bit i960CA processor, a second-generation 80960 developed for embedded systems applications, is the first superscalar microprocessor. The i960CA decodes four and executes three separate instructions per clock cycle. Multiple instruction processing reputedly allows the 33-MHz processor to achieve sustainable throughput of 66 native MIPS.

According to the company, the i960 features a superscalar architecture, code and register file caches, fast data RAM, a flexible system bus interface, a high-speed channel processor with four DMA channels, and a low-latency interrupt control unit. The chip contains almost 600,000 transistors.

Functional units include an integer unit for math and logical operations, a multiply/divide unit, an address generation unit, a bus interface unit, and a parallel instruction scheduler with a data RAM.

The i960CA comes in a 168-pin ceramic PGA in three speed versions. It costs (in 1,000s) $219 for the 16-MHz version, $297 for the 25-MHz version, and $325 for the 33-MHz version. Plastic quad flatpack packaging is scheduled for the second quarter of 1990.

Intel's development tools for the i960CA include the DOS-hosted iC-960 optimizing C Compiler and ASM-960 Macro Assembler; DB-960 Source-Level Debugger; SIM-960 CA Performance Simulator; ICD-960 CA In-Circuit Debugger; and EV80960CA Evaluation Board.

The iC-960 C Compiler costs $3,750 for the MicroVAX/VMS version, $7,500 for the VAX/VMS version, $1,550 for the Sun-3/Unix version, and $700 for the DOS version.

The ASM-960 Macro Assembler costs $3,750 for the MicroVAX/VMS version, $9,500 for the VAX/VMS version, $1,950 for the Sun-3/Unix version, and $900 for the DOS version.

The company says that the iC-960 C Compiler and ASM-960 Macro Assembler are scheduled for availability in December 1989.

The company has also introduced a 1-Mbit burst-access mode EPROM to support the burst-access interface of the i960CA. The 27960CX comes in three speed versions. It is organized 128K × 8 and comes in 44-lead surface-mount plastic leaded chip carriers and 44-lead reprogrammable ceramic quad flatpacks. Samples are available now, with production scheduled for the first quarter of 1990. Prices (in 100s) are $39 for a 16-MHz version, $57 for a 25-MHz version, and $69 for a 33-MHz version in ceramic quad flatpacks. PLCC versions cost $21, $31, and $37, respectively.

i960: **Reader Service 38**
Tools: **Reader Service 39**
EPROM: **Reader Service 40**

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**Reader Service Number 7**

## Program creates systems at the design level

International Consulting Enterprises claims that its Applaud software, Release 2.00, permits developing and maintaining multiuser, PC-based systems at the design level, without programming.

According to ICE, users can build application systems by constructing reusable components. Applaud's screen generator and screen painter assist creation of on-line data entry and inquiry applications. Also available are five types of report generators, the ability to create spreadsheet-style inquiry screens into Applaud databases, import and export of files, and a calculation feature.

Users can also call existing Cobol and C subroutines from within their applications.

Applaud systems function in both single-user and multiuser mode without changes to the software. The program interprets the application's design specifications and automatically inserts record- and file-locking where required.

Applications created with Applaud contain windowing, highlighted bar menus, end-user screen color control, password security, context-sensitive help, and hot-key inquiry into related databases. The software also provides runtime options.

Applaud reportedly creates documentation automatically, based on the design specifications. The end-user manual includes sample reports and screens, data-entry edit rules, and runtime procedures. The system-wide technical documentation includes a data dictionary, database specifications, detailed application specifications, and a system-wide cross-reference list.

Applaud also allows users to create tutorials and demonstrations to accompany their applications.

Applaud requires an IBM PC, XT, AT, or PS/2 or compatible with DOS version 3.0 or higher and a minimum of 640 Kbytes (with 485 Kbytes available for the program). It requires at least one disk drive and a hard disk adequate to run applications plus 3 Mbytes for the Applaud software. Multiuser operation is possible on networks compatible with Novell's Btrieve/N.

Applaud costs $2,495. There are no runtime fees. A free demo is available by calling (800) 426-0428 or (312) 454-3200.

**Reader Service 41**

## ELM implements per-user licensing

Elan Computer Group offers ELM, or Elan License Manager, on Unix platforms. When integrated with a software application, the floating-license manager implements per-user licensing by limiting application access to a specified number of concurrent users.

According to the company, ELM's features include automatic control and administration of per-user floating licensing, the ability to "time bomb" software for creating time-limited evaluation copies, copy guarding, and the ability to license individual features of an application.

Elm costs $7,500 for binary code and $20,000 for source code. Demos are available.

The company is offering the software at the reduced introductory price of $4,500 and $12,000, respectively, until December 15, 1989. Contact ELM Sales at (415) 964-2200, or fax (415) 964-8588.

**Reader Service 42**

At GTE's Computer and Intelligent Systems Laboratory, we are creating opportunities to apply new ideas to research and development projects for improved information and telecommunication systems. By expanding our scope and responsibility, we can better support GTE's telecommunications businesses. And our activities create challenges for individuals at the MS/PhD level in Computer Science. Join us as we continue to make history in telecommunications technology.

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**Intelligent Database Systems**

Our Distributed Object Management (DOM) project is conducting research into interconnectivity and intelligent interoperability among heterogeneous computer systems. We require PhD-level researchers at all levels with a minimum of 2 years' experience in databases, operating systems, distributed systems or artificial intelligence.

**Software Reusability**

Topics of interest in the area of software reusability include domain analysis, object-oriented development, reuse centered software processes, tools support for reusability and software classification. This area requires an MS/PhD in Computer Science and a minimum of 2 years' experience in at least one of the above areas.

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## Graphics workstation fits on a desk

Tektronix has announced the XD88/10 RISC-based graphics workstation, which reportedly achieves 17-MIPS performance. The desktop system includes a color monitor, 156-Mbyte hard disk drive, and 8 Mbytes of RAM for a base price of $15,450. RAM is expandable to 32 Mbytes and disk storage to 3 Gbytes. A VME slot is available. The standard 256-color system is expandable to 24 bit planes with an 8-bit overlay.

The XD88/10 supports the company's implementation of X Window System 11.3 and runs all software ported to X11 on its other XD88 or 4319 workstations. The new system also runs software written to the company's Onramp graphics software library.

The XD88/10 will ship in the first quarter of 1990.

**Reader Service 43**

## IBM offers Application System/Entry models

IBM has announced three Application System/Entry models based on its System/36 5363 System Unit. They use the same operating system and packaging and support the same communications and connectivity options.

The new models incorporate the same disk storage technology used on the AS/400 Models B10 and B20. Each AS/Entry model can reportedly use 1 or 2 Mbytes of memory; the Model S22 handles up to 1.2 Gbytes of disk storage.

Prices range from $11,000 for the AS/Entry Model S10 with 1 Mbyte of memory and 105 Mbytes of disk storage to $36,525 for the Model S22 with 2 Mbytes of main memory and 1.2 Gbytes of disk storage.

**Reader Service 44**

Scientists & Engineers

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## TurboCASE runs on the Macintosh

StructSoft has released TurboCASE for the Apple Macintosh. The software supports Yourdon-DeMarco structured analysis, Gane-Sarson structured analysis, McMenamin and Palmer essential systems analysis, Chen entity relationship modeling, Hatley-Pirbhai real-time modeling, Ward-Mellor real-time modeling, and ESML real-time modeling.

TurboCASE supports a variety of diagram styles, including dataflow diagrams, entity relationship diagrams, structure charts, state transition diagrams, decision tables, minispecifications, flowcharts, and organization charts.

According to the company, the software incorporates automation for such techniques as event partitioning by abstracting a group of processes in a bottom-up approach and implementing intelligent decision tables for process specifications.

The software features object-oriented pop-up menus. Moreover, the data dictionary is integrated with the diagrams and methodologies, so potentially reusable information prompts a dialog box to pop up with appropriate selections.

TurboCASE costs $995. An introductory version is $495, while a demo costs $15.

**Reader Service 45**

## New models join real-time computer family

Concurrent Computer has added the Microthree MPS and Microfive MPS to its Micro3200 family of real-time computers. The new models are compatible with the Series 3200 line.

According to the company, the Micro3200's multiple register sets permit the CPU to respond to high-priority interrupts in 15 microseconds. The OS/32 operating system reportedly allows real-time operations to proceed in parallel with general computational processing on a single multiprocessor configuration.

The Microthree MPS costs $180,000 for two 3.9-MIPS processors, 16 Mbytes of main memory, 20-Mbyte/s I/O throughput, and cabinet. A similarly configured Microfive MPS with two 6.8-MIPS processors costs $260,000.

**Reader Service 46**

## HP mini targets transaction processing

Hewlett-Packard's new high-end HP 3000 Series 960 minicomputer targets the on-line transaction-processing market, according to the company. The Series 960 incorporates HP's RISC-based Precision Architecture and runs the MPE/XL operating system. It costs $485,000. Series 955 owners can upgrade to a Series 960 for $125,000.

The minicomputer features a 15-MIPS CPU with a 37-ns CPU cycle, according to the company, and supports up to 600 users. Main memory is 128 Mbytes standard, expandable to 256 Mbytes. The Series 960 comes with a floating-point coprocessor.

Also standard are a battery backup and automatic restart, IEEE 802.3 LAN terminal connection, and network and relational database-management systems.

**Reader Service 47**

## Terrier adds multitasking to DOS

Visilab Oy claims that its Terrier software enables multitasking in concurrent and real-time PCs using plain MS-DOS. Programming takes place in C, and Terrier services are callable as standard library functions. The resulting program starts in DOS, executes using its services, and returns to DOS.

Development requires either Borland Turbo C (v. 1.5 or later) or Microsoft C (v. 4.0 or later) plus a text editor. Programmers can also code in Turbo Assembler or Microsoft Macro Assembler.

The multitasking feature is limited to one program, in which you can install, awaken, put to sleep, and stop tasks dynamically. The maximum number of tasks is 64, each with its own priority. Programmers can design their own methods of synchronization, protection, and message passing.

Terrier reportedly reserves 1 Kbyte of stack memory for each task, while internal data structures reserve 20 Kbytes of static data. The final program requires 140 Kbytes minimum.

Terrier costs $350, plus $15 freight charges.

**Reader Service 48**

## Computers communicate with telephones

Suncoast Systems offers an intelligent peripheral called Computerfone III that can accept, digitize, store, and transfer incoming speech; dial telephone numbers; answer incoming calls; and convert incoming tones to standard ASCII characters for processing.

The modem-size device also handles operator notification, external switch recognition, and remote contact closing. Optional features include precision call progress, special information tones recognition, a digital modem, and up to 1 Mbyte of expandable memory.

According to the company, Computerfone offers universal adaptability. It can operate with any type of operating system or computer using standard RS-232 or ASCII protocol.

The basic Computerfone III unit costs $695. Call the company's demonstration line at (904) 476-5742.

**Reader Service 49**

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Reader Service Number 8

## IBM offers entry-level fault-tolerant processors

IBM has announced entry-level models in its System/88 line of fault-tolerant processors. The 4593 Integrated Entry System models are software-compatible with the System/88 line.

Features of the new systems include duplexed 16-MHz Motorola 68030 microprocessors; a 32-bit architecture; duplexed memory options of 8, 16, 24, or 32 Mbytes; duplexed DASD options of 152, 319, or 638 Mbytes; a 150-Mbyte quarter-inch cartridge tape; an I/O subsystem with up to 20 workstation ports; and dual power supplies with battery backup.

The 4593 Integrated Entry System will be available in the first quarter of 1990. The base model will cost $48,800 with 8 Mbytes of main memory and 152 Mbytes of DASD memory.

**Reader Service 50**

## Prime adds Sparc workstations

Prime Computer has added three systems to its Sparc-based line of engineering workstations. The new computers are compatible with the company's line of CADDStations, CADDServers, and CADDS software.

Prime will market the workstations as CADDStations when sold with CADDS software or as upgrades to CADDS systems. When sold with Medusa or electronics CAE, CAD, or CAM software, the workstations will be marketed as the WS40C, WS42C, and WS45S.

The WS42C workstation features 12.5 MIPS of processing power, according to the company. It includes a 20-MHz Sparc CPU, a 20-MHz floating-point processor, 12 Mbytes of main memory expandable to 16 Mbytes, and a 19-inch color monitor. It also has an Ethernet controller, a 327-Mbyte SCSI disk drive expandable to 654 Mbytes, a 1.44-Mbyte 3.5-inch floppy disk drive, and a PC MS-DOS emulator. Prices start at $22,660.

The WS40C workstation features a 10-MIPS, 16.67-MHz Sparc CPU, a 20-MHz floating-point coprocessor, 16 Mbytes of main memory expandable to 32 Mbytes, and a 19-inch color monitor. It also includes a 327-Mbyte SCSI disk expandable to 1 Gbyte, a 128-Kbyte cache memory, and a graphics accelerator supporting PHIGS. Prices start at $89,900.

The WS45S server includes a 16-MIPS Sparc CPU, 32 Mbytes of main memory expandable to 56 Mbytes, and a 688-Mbyte hard disk expandable to 5.6 Gbytes. Prices start at $62,800.

Upgrades to the new systems are available.

**Reader Service 51**

**Prime Computer's WS42C relies on Sun Microsystems' Sparc technology.**

## NCR bases systems on 386SX

NCR has based two new desktop systems on Intel's 16-MHz 80386SX microprocessor. The PCs include 16-bit enhanced graphics, advanced disk drive controllers, and on-board memory expansion capabilities. One of them uses Micro Channel Architecture, while the other uses AT bus architecture.

The PC386SX includes 1 Mbyte of RAM, Super VGA adapter, either a 1.2-Mbyte 5.25-inch or 1.44-Mbyte 3.5-inch floppy disk drive, and keyboard for $3,195. A 40-Mbyte hard-drive system costs $4,195, while a 100-Mbyte hard-drive system costs $4,895.

The PC386SX/MC comes with a SCSI hard disk controller that supports up to seven peripherals. A basic model includes 1 Mbyte of RAM, Super VGA support, a 1.44-Mbyte 3.5-inch floppy disk drive, and keyboard for $3,145. A model with a 44-Mbyte SCSI hard disk drive costs $3,895. Systems with 1.44-Mbyte 3.5-inch floppy disk drives and 44- or 100-Mbyte SCSI hard disk drives, Super VGA adapter, and 4-Mbyte RAM costs $5,595 and $6,345, respectively.

**Reader Service 52**

## New Smalltalk/V works with PM

Digitalk has released a version of its Smalltalk/V to work with Presentation Manager. The software provides access to all PM objects, including windows, menus, dialog boxes, and scroll bars. Moreover, applications written in other Smalltalk/V environments can be ported to Smalltalk/V PM.

Smalltalk/V PM generates stand-alone native code applications, requiring no runtime license fees; is portable to DOS and Apple Macintosh versions; comes with a source-level debugger with the ability to set breakpoints, single-step through code, and inspect and change objects; has tools for organizing and browsing Smalltalk source code; and runs on IBM PC, AT, PS/2, or compatible systems with 80286 or 80386 processors and OS/2 Presentation Manager Version 1.1 or later.

The software also features the ability to call any DLL routine, dynamic data exchange, integration with other languages, object inspectors, a tutorial, floating-point emulation, multitasking, a bit editor and free drawing windows, and source code.

Smalltalk/V PM costs $499.95.

**Reader Service 53**

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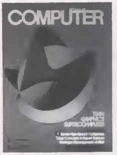

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# IC Announcements

| Company, Model, Function | Comments | R.S. No. |
|---|---|---|
| Analog Devices<br>AD1330<br>DAS | A floating-point data acquisition system in two hybrid packages. Delivers an 18-bit dynamic range A/D conversion. Produces two output words, plus an 18-bit dynamic-range result upon multiplication. Max sample rates to 100 kHz. Comes in a 32-pin and a 48-pin ceramic DIP over KD or TD temperature ranges. Cost (100s): $310 (KD); $620 (TD). | 120 |
| Fujitsu Microelectronics<br>E30000VH<br>Gate array | First in a family of ECL gate arrays. Has gate speeds of 80 ps (typical) unloaded and 240 ps loaded with a fanout of 3 and a line length of 3 mm. Clock skew to internal gates of less than 150 ps. Gate counts from 29,568-38,948 depending on application. Has 300 I/O pins. Comes in a 441-pin ceramic PGA. Sampling in first quarter 1990. Cost (10,000s): $1,600. | 121 |
| Fujitsu Microelectronics<br>MB86232<br>DSP | A 32-bit general-purpose digital signal processor that operates in the IEEE 754 floating-point data format. Also supports 32-bit fixed-point and 24-bit integer formats. Has a three-port RAM block, dual internal data buses, and dual accumulators. Comes in a 208-pin ceramic PGA. Cost: $1,200 (engineering samples). | 122 |
| Gemini Technology<br>VC-002, VC-003<br>VGA controllers | VGA video controller chips. VC-002 drives analog, digital, or gas plasma video monitors in 8- and 16-bit bus computers for 800 × 600 extended VGA resolution in 256 colors. VC-003 adds standard 640 × 480 VGA resolution with 16 colors or shades of gray for LCD-based video screens. Cost (samples): $45 for VC-002; $55 for VC-003. | 123 |
| Hitachi America<br>HM571000JP<br>DRAM | A 1-Mbit DRAM with an access time of 45 ns. Has 16 address pins. Runs on a 5V supply and draws a max of 120 mA. Organized 1 Mbit × 1 (available 256 Kbit × 4 as the HM574256JP-45). Comes in a 28-pin SOJ. Cost (1,000s): $65 (engineering samples). | 124 |
| LSI Logic<br>LEA100K<br>Embedded arrays | An ASIC family of Channel-Free Compacted Array Plus devices into which user-defined megacells or memory can be embedded. Allows designs up to 150,000 equivalent gates using combined cell- and array-based methods. Netlist and library compatible with other LSI Logic devices. Cost: varies. | 125 |
| LSI Logic<br>L64853<br>DMA controller | A direct memory access controller for the SBus architecture developed by Sun Microsystems. Features a two-channel DMA controller optimized for SCSI and Ethernet, support for 8- and 16-bit peripherals, and 32-bit byte packing and unpacking. Comes in a 120-pin plastic quad flatpack. Cost (100s): $76 (samples). | 126 |
| Oak Technology<br>Oak Horizon<br>Laptop PC chip set | A set of five ICs for 286- and 386SX-based laptop PCs. Includes OTI-051 System Controller, OTI-052 I/O Peripheral Controller, OTI-053 DMA and Memory Controller, OTI-054 Address Buffer/Real-time Clock, and OTI-055 Data Buffer/Power Manager. Comes in 100-pin plastic quad flatpacks. Cost (1,000s): $90. | 127 |
| Phillips Components-Signetics<br>27C210<br>EPROM | A 1-Mbit EPROM organized 65,536 words × 16 bits. Offered at a $T_{AA}$ of 200 ns. Uses the Quick Pulse Programming Algorithm. Inputs controlled by the active low output enable. Comes in 40-pin windowed ceramic and plastic DIPs, plus 44-pin PLCCs. Cost (100s): $25.75 (windowed ceramic DIP); $20.40 (plastic DIP); $22.90 (PLCC). | 128 |
| Sony<br>CXK7701J<br>Cache memory | A 32-Kbyte, two-way, set-associative cache memory. Works with the Intel 80386 CPU and 82385 cache controller. Combines the functions of address latch, memory, and transceiver into one or two ICs. Configurable as an 8K × 16-bit memory or as two 4K × 16-bit memories. Comes in 52-pin PLCCs. Cost: $49.50 (samples). | 129 |
| Sony<br>E3G70<br>Gate array | A 70-gate, 100-ps per gate emitter-coupled logic array, part of the SPECL family. Designed for applications requiring 3-GHz operating speed or a small skew. Obtainable in 24- or 32-pin flat metal packages. Cost (1,000s): $50; $33,000 for nonrecurring engineering fee. | 130 |
| Tseng Laboratories<br>ET4000<br>VGA controller | A VGA controller chip for IBM PC, XT, AT, PS/2, and compatibles offering register-level compatibility in video standards using VGA, EGA, CGA, MDA, and Hercules modes. Available separately or in adapter configurations. Now sampling. Prices not set. | 131 |
| Vermont Microsystems<br>VCAD<br>Graphics chip | A Video Control and Drawing graphics accelerator chip for the Intel i860 RISC processor. Draws 400,000 10-pixel vectors per second. Controls 1-Mbyte VRAM devices in frame resolutions up to 1,280 × 1,024 and 24 bit planes. Cost (1,000s): $105. | 132 |

# Microsystem Announcements

| Company, Model, Function | Comments | R.S. No. |
|---|---|---|
| Analogic/CDA<br>MDP-6E<br>Image processor | A Sun-3/E compatible image processor system with a 20 Mflops peak rate. Integrates imaging, graphics, and text. Consists of three 6U VME cards: SMB-6E Screen Memory Board; MSP-6 32-bit array processor; and optional image memory board. Interfaces to the Sun P2 graphics bus. Cost: around $16,000 (OEM quantities). | 135 |
| Arcom Control Systems<br>SCPC286<br>SBC | An AT-PS/2 compatible computer on the STEbus on a single Eurocard. Includes a 12-MHz 80286, a VLSI implementation of AT-PS/2 logic, sockets for 1 Mbyte of RAM (0.5 Mbyte standard), sockets for EPROM and an 80287, disk and keyboard/mouse interfaces, a loudspeaker, and a battery-backed real-time clock. Cost: £695. | 136 |
| Astro Systems<br>Traveller Drive System<br>Removable hard drive | A 3.5-inch removable hard disk drive compatible with desktop and laptop computers. Consists of three modules: Travelpak, Travelport, and an adapter card. Travelpak comes with 40, 80, or 100 Mbytes and has an average seek time of 19 ms. Travelport includes cables and the appropriate adapter card. Cost: $1,125-$2,715. | 137 |
| Hyperspeed<br>Single- and Dual-860<br>Coprocessors | Coprocessor boards based on Intel's 64-bit 80860. Single-860 uses a 33-MHz 80860, 2 or 4 Mbytes of DRAM expandable to 8 or 16 Mbytes, AT bus interface, and Master Mode access of PC memory and I/O ports. Cost: $7,500 for Single-860 with 2 Mbytes. | 138 |
| Kontron Electronics<br>PLA/2<br>Logic analyzer | An AT-based logic analyzer with up to 192 channels at 50 MHz synchronous, 100 MHz asynchronous, or 200 MHz asynchronous in interlace mode. Uses transitional timing for all channels across memory depths of 4K or 16K. Triggering circuitry allows real-time cross-link between state and timing events. Cost: starts at $14,995. | 139 |
| Micro Industries<br>MIB II 960/110<br>Development board | A RISC development board based on Intel's i960CA microprocessor and Multibus II. Includes the i960CA, a configuration processor, a message-passing coprocessor, a socket for a boot EPROM, 1 Mbyte of DRAM, 64 Kbytes of SRAM, an 8254 programmable interval timer, and an 82510 UART. Cost: $5,000. | 140 |
| Network Resources<br>Mac2000<br>Communications card | A NuBus expansion card that connects Apple Macintosh II computers to Ethernet, broadband, or fiber-optic networks. Based on Apple's Mac Coprocessor Platform. Includes a 10-MHz Motorola 68000, 512 Kbytes of RAM, and an on-board transceiver. Cost: $995. | 141 |
| Number Nine Computer<br>Pepper Pro1024<br>Graphics boards | A family of graphics boards based on TI's 60-MHz TMS34010. Compatible with IBM Micro Channel and AT/XT bus architectures. Features 1,024 × 768 noninterlaced resolution with up to 256 colors from a 16.7-million palette. Comes with 1.5 Mbytes of memory per board. Direct bitmap support of Intel's 80x86 processors. Cost: $2,495. | 142 |
| Tadpole Technology<br>TP960V<br>SBC | A VMEbus single-board computer based on Intel's 80960CA processor. Variable configurations available. Max memory of 512 Kbytes of SRAM and 16 Mbytes of dual-ported DRAM, plus up to 1 Mbyte of flash EPROM. All options come with the TPROM monitor and diagnostic firmware. Cost: varies according to configuration. | 143 |
| Tadpole Technology<br>TP860M<br>SBC | A single-board computer based on Intel's 80860 64-bit RISC processor. Provides one to three 80860 processors with memory, SCSI controller, Ethernet interface, and 3D color graphics subsystem with 1,280 × 1,024 resolution. Comes in 6U extended Eurocard or Multibus II formats. Second quarter 1990. Prices not set. | 144 |
| Telesystems<br>ARLAN 450<br>PC LAN card | A wireless LAN card that plugs into IBM PCs or compatibles and runs under Novell Netware. Includes a data-packet radio and network access unit. Approved under FCC part 15 for use without radio license. Has a 230-Kbps transmission rate. Cost: $800-$1,500. | 145 |
| Touchbase Systems<br>Worldport 2400/MNP<br>External modem | A portable external modem that supports the Microcom MNP Class 5 standard. Features error correction, data compression, 2,400-bps data speed, battery power, compatibility with Bell and CCITT protocols, and telephone connection through both direct connect and acoustic couplers. Cost: $499. | 146 |
| Verbex Voice Systems<br>Model 0500<br>Voice I/O board | A conversational voice I/O board, a single-board version of the Series 5000. Includes speech recognition, voice response, and I/O control. Also configurable in a multiline controller or daisy-chained on a single line. Includes a TI TM320 DSP, a Verbex gate array, a Motorola 68000, and an Intel microprocessor. Cost: starts around $3,000. | 147 |

IEEE TRANSACTIONS ON

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**A PUBLICATION OF THE IEEE COMPUTER SOCIETY**

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Hardware/software issues and applications studies specifically for parallel and/or distributed systems.

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**FIRST ISSUE:** January 1990 **FREQUENCY:** Quarterly

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## SCOPE:

Hardware/software issues and applications studies specifically for parallel and/or distributed systems.

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## SAMPLE SUBJECT AREAS:

**Parallel and distributed architectures** — Design, analysis, and implementation of multiple-processor systems; impact of VLSI on parallel/distributed design; inter-processor/memory communications.
**Parallel and distributed software** — Parallel languages and compilers; scheduling and task partitioning; databases in parallel/distributed systems.
**Parallel algorithms and applications** — Parallel models of computation; analysis and design of parallel numeric/non-numeric algorithms; applications studies using parallel/distributed systems.
**Other issues** — Performance measurements, evaluation, modeling and simulation of parallel/distributed architectures; reliability and fault-tolerance issues concerning parallel/distributed systems.

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## DeConcini to keynote Fifth Computer Security Applications Conference

Senator Dennis DeConcini (D-Ariz.), a member of the US Senate Appropriations and Judiciary Committees and the Select Committee on Intelligence, will deliver the keynote address when the Fifth Computer Security Applications Conference convenes in Tucson, Arizona, December 4-8.

The event is sponsored by the American Society for Industrial Security and Aerospace Computer Security Associates in cooperation with the IEEE Computer Society Technical Committee for Privacy and Security.

The conference will explore technology applications in complementary aspects: the policy issues and operational requirements for civil and military systems; the hardware and software tools and techniques being developed to satisfy system requirements; and specific examples of systems applications and implementations. The technical and research portion of the conference will feature a mix of panels and paper presentations on varied topics, including computer crime, human issues, network security, database security, policy and standards, risk management, security architecture, and integrity.

During the conference, Steven T. Walker will be honored as the first recipient of the Distinguished Lecturer Award, initiated by Aerospace Computer Security Associates. Walker will be recognized for major contributions to the computer security field and, in turn, will present a talk entitled "Infosec: Where Are We Going?"

Walker, known for his pioneering work on the US Department of Defense Computer Security Initiative, established the National Computer Security Center and has extensive experience in the design and implementation of large-scale computer networks and information systems. He is the founder and president of Trusted Information Systems, a small business specializing in computer and communications security techniques.

Walker received the National Computer System Security Award in 1988 and is a member of the Defense Science Board Task Force on the Defense Data Network.

Charles T. Force, NASA associate administrator for space operations, and Dave Fitzsimmons, Arizona Daily Star editorial cartoonist, will speak at luncheons December 6 and 7, respectively.

Force manages NASA's worldwide tracking, data, and communications networks, which support all manned spacecraft, unmanned satellites, and interplanetary probes. He is also responsible for advising NASA's administrator and deputy administrator on the overall organization of operations within the agency.

For more information, call Diana Akers at (703) 883-5907 or Victoria Ashby at (703) 883-6368, or write them at Mitre, 7525 Colshire Dr., McLean, VA 22102.

## Hardware verification workshop proves need for continuing forum, say organizers

*Teresa Craighead, Cornell University*

A workshop on "Hardware Specification, Verification, and Synthesis: Mathematical Aspects" attracted 75 electrical engineers and computer scientists to Cornell University for an unusual opportunity to address current research in the field of VLSI design verification and synthesis.

Cornell's Geoffrey Brown and Miriam Leeser organized the July 5-7 workshop, sponsored by the Mathematical Sciences Institute, which is partially funded by the US Army Research Office. Brown and Leeser said the relatively large turnout proved the need for an annual forum on this topic in North America.

Steve Johnson of Indiana University described the event as "one of the only forums available addressing this aspect of VLSI design." Johnson said that "established workshops in Europe contribute to European leadership in this new area by accelerating the dissemination of ideas and methods."

Spurred by the need for more reliable hardware, especially in remote systems intolerant of failure, and the realization that theorem provers have been successfully applied to the design of reliable computer programs, researchers are looking for ways to prove the validity of computerized hardware design and synthesis tools. Success in this research could lead in five to 10 years to more reliable circuits and tools for less sophisticated hardware designers who need to rely on foolproof methods.

George Milne, University of Strathclyde, a leader in the field and one of the workshop's invited speakers, said, "The workshop tackled the complex problem of verifying hardware through complex verification proofs." He urged attendees to focus research on the issues of integrating design and verification, verifying design synthesis, and designing for verifiability.

Milne emphasized that research in these areas is difficult because few scientists have the necessary background in both theoretical computer science and hardware design.

Brown and Leeser have expertise in both areas. Milne termed their work "original" and said they are among the few focusing their research in the directions he advocates.

"Scientists at the workshop seemed to acknowledge the need to integrate proof-oriented methods with synthesis and the need to automate more mundane aspects of circuit verification," Johnson said. He said he feels a basic issue remains open and asked, "Where do we stop trying to apply formal methods to physical structures?" "Can physical structures realize the abstractions we are imposing on them?" and "Where should a formal, logical view of electronics set its frontier?" These issues should be considered simultaneously with those surrounding the mechanics of verification and synthesis, he added.

# Call for Papers
## 1990 ACM International Conference on Supercomputing

**June 11-15, Amsterdam, the Netherlands**
(Vrije Universiteit and Centrum voor Wiskunde en Informatica)

**Sponsored by ACM SIGARCH**
in association with AICA, BCS-PPG, CTI, CSRD, CWI,
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**Conference Co-Chairmen**
Ahmed Sameh, Univ of Illinois Center for Supercomputing R&D, USA
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**Program Director**
John R. Sopka, Digital Equipment Corporation, USA

The fourth ACM International Conference on Supercomputing is now soliciting papers on significant new research results in the development and use of supercomputing systems. Contributions should emphasize the novel aspects of the work being reported and should discuss their implications for future supercomputing development. Submissions are solicited in the following areas:

- Architectural Design of Supercomputing Systems, including:
  - Heterogeneous use of MIMD, SIMD and Data Flow Systems Designs,
  - Memory System Organization (Distributed, Shared or Hierarchical),
  - Bus, Network and Communication Systems, Data Storage and Access.
- Software Systems Support for Supercomputing, such as:
  - Operating Systems Support Features,
  - Programming Languages, Compilers and Analysis Tools,
  - Programming Environments and High Level Problem Solving Systems.
- Applications of Supercomputing, including:
  - Computational Fluid Dynamics, Computational Chemistry,
  - Structural Mechanics, Graphics and Visualization,
  - Circuit and Semiconductor Device Simulation,
  - Artificial Intelligence and Symbolic Computation,
  - Other new or nontraditional applications.
- Supercomputing Algorithms and Performance Analysis, for example:
  - Highly Parallel Numerical and Non-Numerical Algorithms,
  - Performance Evaluation Tools, Methods and Modeling,
  - Supercomputing System Benchmarking and Performance Studies.

Conference proceedings, published by Springer-Verlag in 1987 and ACM in 1988 and 1989, will again be published by ACM in 1990. Authors should send five (5) copies of the manuscript to the program chair for their region. The deadline for submissions is January 10, 1990. Authors will be notified of acceptance by March 10, 1990. Final versions of accepted submissions will be due by April 15, 1990.
The addresses for submissions are:

Program Chair for
Europe and Africa:
**Dr. John R. Gurd**
Dept. of Computer Science
Univ. of Manchester
Oxford Road
Manchester M13 9PL
UNITED KINGDOM
jgurd@uk.ac.man.cs.ux

Program Chair for
North and South America:
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Univ. of Illinois CSRD
305 Talbot Laboratory
104 South Wright St.
Urbana, IL 61801-2932
USA
stratis@uicsrd.csrd.uiuc.edu

Program Chair for
Japan and the Far East:
**Dr. Yoichi Muraoka**
Dept. of Elect. Eng.
Waseda University
3-4-1 Okubo, Shinjuku-ku
Tokyo
JAPAN
muraoka@jpnwas00.bitnet

# CALL FOR PAPERS

**Conf. on AI, Simulation, and Planning in High-Autonomy** Systems: Mar. 26-27, Tucson, Ariz. Cosponsors: Univ. of Arizona et al. Submit abstract by **Nov. 17, 1989,** to Office of Engineering Professional Development, Univ. of Arizona, Box 9 Harvill Bldg., Tucson, AZ 85721, phone (602) 621-3054.

**17th Int'l Symp. on Computer Architecture:** May 28-31, 1990, Seattle. Cosponsor: ACM. Submit paper by **Nov. 21, 1989,** to James Goodman, Computer Sciences Dept., Univ. of Wisconsin, 1210 W. Dayton, Madison, WI 53706, phone (608) 262-1204.

**Flairs 90, Florida AI Research Symp.:** Apr. 3-6, 1990, Cocoa Beach, Fla. Submit abstract by **Nov. 27, 1989,** to Douglas D. Dankel II, Flairs 90, E301 CSE, C.I.S., Univ. of Florida, Gainesville, FL 32611, phone (904) 335-8034.

**IMSC 90, Int'l Mobile Satellite Conf.:** June 18-20, 1990, Ottawa, Canada. Cosponsors: NASA, Canadian Dept. of Communications. Submit synopsis by **Nov. 30, 1989,** to IMSC 90 Organizing Committee, c/o D. Hugh M. Reekie, Dept. of Communications, 300 Slater St., Ottawa, Ont., Canada, K1A 0C8.

***IEEE Trans. on Knowledge and Data Engineering*** plans a special section on knowledge engineering and software engineering. Submit paper by **Dec. 1, 1989,** to S.K. Chang, Computer Science Dept., Univ. of Pittsburgh, Pittsburgh, PA 15260, phone (412) 624-8490.

**Coling 90, 13th Int'l Conf. on Computational Linguistics:** Aug. 20-25, 1990, Helsinki, Finland. Submit paper by **Dec. 1, 1989,** to Hans Karlgren, KVAL, Skeppsbron 26, S-111 30 Stockholm, Sweden, phone 46 (8) 789-6683.

**Third Int'l Conf. on Industrial and Engineering Applications for AI and Expert Systems:** July 15-18, 1990, Charleston, S.C. Cosponsors: ACM et al. Submit extended abstract by **Dec. 1, 1989,** to Manton M. Matthews, Computer Science, Univ. of South Carolina, Columbia, SC 29208, phone (803) 777-3285.

**1990 ACM Conf. on Lisp and Functional Programming:** June 27-29, 1990, Nice, France. Submit paper by **Dec. 1, 1989,** to Mitchell Wand, Attn. LFP 90, College of Computer Science, 169 Cullinane Hall, Northeastern Univ., Boston, MA 02115, phone (617) 437-3539.

**43rd SPSE Conf.:** May 20-25, 1990, Rochester, N.Y. Sponsor: Society for Imaging Science and Technology. Submit abstract by **Dec. 1, 1989,** to Rodney Shaw, Rochester Inst. of Technology, Center for Imaging Science, 1 Lomb Memorial Dr., Rochester, NY 14623.

**1990 SID Int'l Symp.:** May 14-18, 1990, Las Vegas. Submit abstract by **Dec. 1, 1989,** to Lynne Henderson, Society for Information Display, Palisades Inst. of Research Services, 201 Varick St., Suite 1140, New York, NY 10014, phone (212) 620-3375.

**Iberamia 90, Second Ibero-American Conf. on AI:** July 9-13, 1990, Morelia, Michoacan, Mexico. Sponsors: Centro Regional de Ensenanza en Informatica (Spain) et al. Submit paper in Spanish or Portuguese by **Dec. 1, 1989,** to Iberamia 90, Atn. Srita. Ma. Antonieta Alvarez Perez, Apartado Postal 70302, C.P. 04510, Mexico, D.F.

**19th Mumps Users' Group Meeting:** June 11-15, 1990, Orlando, Fla. Submit paper by **Dec. 1, 1989,** to Mumps Users' Group, 4321 Hartwick Rd., Suite 100, College Park, MD 20740, phone (301) 779-6555.

***J. of Parallel and Distributed Computing*** plans a special issue in December 1990 on dataflow multiprocessing. Submit paper by **Dec. 1, 1989,** to Jean-Luc Gaudiot, Electrical Engineering-Systems Dept., Univ. of Southern California. Los Angeles, CA 90089-0781, phone (213) 743-0249; or Lubomir Bic, Information and Computer Science Dept., Univ. of California, Irvine, CA 92717, phone (714) 856-5248.

**First Int'l Symp. on Environments and Tools for Ada:** Apr. 30-May 2, 1990, Redondo Beach, Calif. Cosponsor: ACM. Submit paper by **Dec. 4, 1989,** to Dewayne E. Perry, AT&T Bell Laboratories, 600 Mountain Ave., Murray Hill, NJ 07974, phone (201) 582-2529.

**ICCC 90, 10th Int'l Conf. on Computer Communication:** Nov. 5-9, 1990, New Delhi, India. Sponsor: Int'l Council on Computer Communication. Submit draft of paper by **Jan. 20, 1990** to S. Ramani, National Centre for Software Technology, Gulmohar Cross Rd. No. 9, Juhu, Bombay 400-049, India, phone 91 (22) 620-1606.

**Eighth Built-In Self Test Workshop:** Mar. 21-23, 1990, Charleston, S.C. Sponsors: IEEE Test Technology Committee, IEEE International Test Conf. Submit abstract by **Dec. 4, 1989,** to Richard Sedmak, Self-Test Services, 6 Lindenwold Terr., Ambler, PA 19002, phone (215) 628-9700.

**IAPR Workshop on Syntactic and Structural Pattern Recognition:** June 13-15, 1990, Murray Hill, N.J. Sponsor: Int'l Assoc. for Pattern Recognition. Submit paper by **Dec. 8, 1989,** and abstract by **Mar. 1, 1990,** to Henry S. Baird, AT&T Bell Laboratories, Rm. 2C-557, 600 Mountain Ave., Murray Hill, NJ 07974, phone (201) 582-5744.

**Compass 90, Fifth Conf. on Computer Assurance: Systems Integrity, Software Safety, and Process Security:** June 26-29, 1990, Gaithersburg, Md. Cosponsors: IEEE Aerospace and Electronics Society, IEEE National Capital Area Council. Submit paper by **Dec. 12, 1989,** to H.O. Lubbes, 13212 Taney Dr., Beltsville, MD 20705, phone (202) 404-7237.

**IAAI 90, Second Conf. on Innovative Applications of Artificial Intelligence:** May 1-3, 1990, Washington, DC. Sponsor: American Assoc. for Artificial Intelligence. Submit paper by **Dec. 12, 1989,** to IAAI 90, AAAI, 445 Burgess Dr., Menlo Park, CA 94025, phone (415) 328-3123.

*IEEE Software* plans a special Software Tools Fair issue in May 1990. Request special form from Paul Oman, Computer Science Dept., Engineering College, Univ. of Idaho, Moscow, ID 83843, phone (208) 885-6589. The submittal deadline is **Dec. 15, 1989.**

**Fourth Parallel Processing Symp.:** Apr. 3-5, 1990, Fullerton, Calif. Cosponsor: California State Univ. at Fullerton. Submit paper by **Dec. 15, 1989,** to Larry H. Canter, c/o Computer Systems Approach, 1140 S. Raymond Ave., Suite B., Fullerton, CA 92631, phone (714) 738-3414.

**1990 IEEE VLSI Test Workshop:** Apr. 10-11, 1990, Atlantic City, NJ. Cosponsor: IEEE Philadelphia Section. Submit abstract by **Dec. 15, 1989,** to Mukund Modi, Naval Air Engineering Center, ATE Software Center, Code: 52514, Lakehurst, NJ 08733, phone (201) 323-7002.

**First Workshop on Neural Networks: Academic/Industrial/NASA/Defense Technical Interchange and Tutorials:** Feb. 5-6, 1990, Auburn, Ala. Sponsors: NASA/Center for Commercial Development of Space Power and Advanced Electronics et al. Submit abstract by **Dec. 15, 1989,** to Mary Lou Padgett, John Wu, or T. Roppel, EE Dept., 200 Broun Hall, Auburn Univ., AL 36849, phone (205) 844-1855.

**CBMS 90, Third IEEE Symp. on Computer-Based Medical Systems:** June 3-6, 1990, Chapel Hill, N.C. Cosponsor: IEEE Engineering in Medicine and Biology Society. Submit summary by **Dec. 15, 1989,** to James N. Brown, Jr., Research Triangle Inst., Box 12194, Research Triangle Park, NC 27709, phone (919) 541-6994.

**AAAI 90 National Conf. on AI Workshop:** July 31-Aug. 3, 1990, Boston. Sponsor: American Assoc. for Artificial Intelligence. Submit proposal by **Dec. 15, 1989,** to Edward Lafferty, AI Center, Mitre, MS A350, Burlington Rd., Bedford, MA 01730, phone (617) 271-2773.

**ACL 90, 28th Conf. of the Assoc. for Computational Linguistics:** June 6-9, 1990, Pittsburgh. Submit paper by **Dec. 16, 1989,** to Robert C. Berwick, MIT AI Lab, Rm. 838, 545 Technology Square, Cambridge, MA 02139, phone (617) 253-8918.

***J. of Systems and Software*** plans a special issue about learning from expert systems projects that failed to meet expectations. Submit paper by **Dec. 31, 1989,** to Larry Travis, Computer Sciences Dept., Univ. of Wisconsin at Madison, 1210 W. Dayton St., Madison, WI 53706, phone (608) 262-6587.

**Advanced Research Workshop on 3D Imaging in Medicine:** June 25-29, 1990, Travemuende, Federal Republic of Germany. Sponsor: NATO. Submit paper by **Jan. 2, 1990,** to Linda Houseman, Computer Science Dept., Univ. of North Carolina, Box 3175, Sitterson Hall, Chapel Hill, NC 27599, phone (919) 962-1758 (for authors in the Americas); or Andreas Pommert, Inst. fur Mathematik und Datenverarbeitung in der Medizin, Univ. Krankenhaus Eppendorf, Martinistrasse 52, 2000 Hamburg 20, Federal Republic of Germany, phone 49 (40) 468-2300 (for authors in Europe, Asia, Australia, and Africa).

**IFIP Workshop on Design and Test of ASICs:** June 11-12, 1990, Hiroshima, Japan. Cosponsors: IPSJ et al. Submit abstract by **Jan. 10, 1990,** to IFIP WG 10.5 Design and Test of ASICs Workshop Secretariat, c/o Business Center for Academic Science Japan, 3-23-1 Hongo, Bunkyo-ku, Tokyo 113, Japan, phone 81 (3) 817-5831.

**ICPP 90, 19th Int'l Conf. on Parallel Processing:** Aug. 13-17, 1990, St. Charles, Ill. Submit abstract and paper according to subject area by **Jan. 10, 1990,** to: Peng-Chung Yew, Center for Supercomputing Research and Development, Univ. of Illinois, 305 Talbot Lab, 104 S. Wright St., Urbana, IL 61801-2932, phone (217) 244-0045 (on algorithms and applications subjects); David A. Padua, Center for Supercomputing Research and Development, Univ. of Illinois, 305 Talbot Lab, 104 S. Wright St., Urbana, IL 61801-2932, phone (217) 333-4223 (on software-oriented subjects); Benjamin W. Wah, Coordinated Science Lab, Univ. of Illinois, 1101 W. Springfield Ave., Urbana, IL 61801-3082, phone (217) 333-3516 (on hardware-oriented and other subjects).

**ITC 90, Int'l Test Conf.:** Sept. 10-12, 1990, Washington, DC. Cosponsor: IEEE Philadelphia Section. Submit paper by **Jan. 15, 1990,** to Birger Schneider, ElektronikCentralen, Venlighedsvej 4, DK 2970 Horsholm, Denmark, phone (45) 42-867722 (for Europe); to Adit Singh, Computer Science Dept., Indian Inst. of Technology, New Delhi, India (for India); or, by **Jan. 22, 1990,** to H. Alan Hoover, ITC, PO Box 264, Mt. Freedom, NJ 07970, phone (219) 895-5260 (for North America); or to Teruo Tamama, NTT LSI Labs, 3-1 Morinosato Wakamiya, Atsugi-Shi, Kanagawa 243-01, Japan, phone (81) 462-40-2225 (for Asia).

**Cognitiva 90:** Nov. 20-23, 1990, Madrid. Sponsor: AFCET. Submit abstract by **Jan. 15, 1990,** to Cognitiva 90, c/o AFCET, 156 Bd Pereire 75017 Paris, France, phone 33 (01) 47-66-24-19.

**Roundtable Discussion on Vision-Based Vehicle Guidance:** July 2, 1990, Tokyo. Sponsor: Committee of IEEE Int'l Workshop on Intelligent Robots and Systems. Submit abstract by **Jan. 15, 1990,** to Ichiro Masaki, Computer Science Dept., GM Research Labs, 30500 Mound Rd., Warren, MI 48090-9055, phone (313) 986-1466.

**Tencon 90, IEEE Region 10 Conf. on Computer and Communication Systems:** Sept. 24-27, 1990, Hong Kong. Cosponsor: IEEE Hong Kong Section. Submit extended summary and abstract by **Jan. 22, 1990,** to Y.S. Cheung, Electrical and Electronic Engineering Dept., Univ. of Hong Kong, Pokfulam, Hong Kong.

**13th Int'l ACM/SIGIR Conf. on Research and Development in Information Retrieval:** Sept. 5-7, 1990, Brussels. Submit paper by **Jan. 31, 1990,** to Gerard Salton, Computer Science Dept., Cornell Univ., 4133 Upson Hall, Ithaca, NY 14853 (for authors in the Americas and Asia); or Leo Egghe, Limburgs Univ. Centrum, Universitaire Campus, B-3610 Diepenbeek, Belgium (for authors in Europe, Africa, and Australia).

**ICARCV 90, Int'l Conf. on Automation, Robotics, and Computer Vision:** Sept. 18-21, 1990, Singapore. Submit extended summary and abstract by **Jan. 31, 1990,** to D.P. Mital, ICARCV 90, School of Electrical and Electronic Engineering, Nanyang Technological Inst., Nanyang Avenue, Singapore 2263.

**Eurographics Workshop on Object-Oriented Graphics:** June 6-8, 1990, Konigswinter, Federal Republic of Germany. Sponsors: Eurographics and German Society for Informatics. Submit paper by **Jan. 31, 1990,** to Marja Hegt, O-O Graphics Workshop, CWI, Kruislaan 413, 1098 SJ Amsterdam, The Netherlands, phone 31 (20) 592-4058.

**21st Pittsburgh Conf. on Modeling and Simulation:** May 3-4, 1990, Pittsburgh. Sponsors: Univ. of Pittsburgh et al. Submit abstract and summary by **Jan. 31, 1990,** to William G. Vogt or Marlin H. Mickle, Modeling and Simulation Conf., 348 Benedum Engineering Hall, Univ. of Pittsburgh, Pittsburgh, PA 15261.

**ISPRS Commission V Symp.:** Sept. 3-7, 1990, Zurich, Switzerland. Cosponsors: Int'l Society for Photogrammetry and Remote Sensing et al. Submit abstract by **Jan. 31, 1990,** and paper by **June 15, 1990,** to ISPRS Commission V Symp., Inst. of Geodesy and Photogrammetry, ETH-Hoenggerberg, 8093 Zurich, Switzerland, phone 41 (1) 377-3051.

**CC 90, Third Int'l Workshop on Compiler Compilers:** Oct. 22-26, 1990, Schwerin, German Democratic Republic. Sponsors: German Democratic Republic Academy of Sciences Inst. of Informatics and Computing Technique et al. Submit preliminary paper by **Jan. 31, 1990,** to CC 90 Organizing Committee, c/o Michael Albinus, Akademie der Wissenschaften der DDR, Inst. für Informatik und Rechentechnik, Rudower Chaussee 5, Berlin, DDR — 1199.

**InfoJapan 90, Int'l Conf. on Information Technology:** Oct. 1-5, 1990, Tokyo. Sponsor: IPSJ. Submit paper by **Feb. 1, 1990,** to Haruhisa Ishida, Computer Center, Univ. of Tokyo, 2-11-16 Yayoi, Bunkyo-ku, Tokyo 113, Japan, phone 81 (3) 818-0287.

**ICCD 90, IEEE Int'l Conf. on Computer Design: VLSI in Computers and Processors:** Sept. 16-19, 1990, Cambridge, Mass. Submit summary by **Feb. 1, 1990,** to Edward M. Middlesworth, Hewlett-Packard, Bldg. 25U, PO Box 10350, Palo Alto, CA 94303-0867, phone (415) 857-5485.

**Second Int'l Conf. on Software Engineering and Knowledge Engineering:** June 21-23, 1990, Skokie, Ill. Sponsors: Knowledge Systems Inst., Univ. of Pittsburgh, and Inst. for Information Industries, Taiwan. Submit abstract and paper by **Feb. 1, 1990,** to C.Y. Hsieh, Computer Science Dept., Knowledge Systems Inst., 1153 Oak St., PO Box 576, Winnetka, IL 60093-0576.

**Int'l Workshop on Rapid System Prototyping:** June 5-7, 1990, Triangle Research Park, N.C. Submit extended summary and paper by **Feb. 15, 1990,** to Nick Kanopoulos, Center for Digital Systems Research, Research Triangle Inst., PO Box 12194, Research Triangle Park, NC 27709, phone (919) 541-7341.

**Int'l Symp. on Algorithms:** Aug. 16-18, 1990, Tokyo. Sponsor: IPSJ Special Interest Group on Algorithms. Submit detailed abstract by **Feb. 15, 1990,** to Tetsuo Asano, Osaka Electro-Communication Univ., Hatsu-cho, Neyagawa, Osaka 572, Japan, phone 81 (720) 24-1131.

**Fifth Jerusalem Conf. on Information Technology:** Oct. 22-25, 1990, Jerusalem Israel. Sponsor: Information Processing Assoc. of Israel. Submit paper by **Feb. 15, 1990,** to Noah Prywes, Computer and Information Dept., Univ. of Pennsylvania, Philadelphia, PA 19104 (for authors in North America); or Amir Pnueli, Applied Mathematics and Computer Science Dept., Weizmann Inst. of Science, Rehovot, Israel (for all other authors).

**EKAW 90, Fourth European Knowledge Acquisition for Knowledge-Based Systems Workshop:** June 25-29, 1990, Amsterdam. Submit paper by **Feb. 26, 1990,** to Bob Wielinga, Social Science Informatics, Univ. of Amsterdam, Herengracht 196, 1016 BS Amsterdam, The Netherlands, phone 31 (20) 525-2160.

***Proc. of the IEEE*** plans a special issue in Jan. 1991 on ISDN. Submit paper on networks, service, systems, performance, switching, standardization efforts, device developments, future trends, and new directions by **Feb. 28, 1990,** to W.W. Wu, Intelsat, 3400 International Dr. NW, Washington, DC 20008-3098, phone (202) 944-7224.

**First Japanese Knowledge Acquisition for Knowledge-Based Systems Workshop:** Oct.

25-26, 1990, Kyoto, Japan, and Oct. 29-31, 1990, Tokyo. Cosponsors: Kansai Inst. of Information Systems et al. Submit draft paper by **Feb. 28, 1990,** to Hiroshi Motoda, Advanced Research Lab, Hitachi, Kokubunji, Tokyo 185, Japan.

**DIAC 90, Directions and Implications of Advanced Computing:** July 28, 1990, Boston. Sponsor: Computer Professionals for Social Responsibility. Submit abstract and paper by **Mar. 1, 1990**, to Douglas Schuler, Boeing Computer Services, MS 7L-64, PO 24346, Seattle, WA 98124-0346, phone (206) 865-3226.

**ICCS 90, Int'l Conf. on Communication Systems:** Nov. 5-9, 1990, Singapore. Cosponsors: IEEE Singapore Section et al. Submit abstract by **Mar. 1, 1990,** to T.T. Tjhung, ICCS 90, c/o Meeting Planners Pte Ltd., 100 Beach Rd. #33-01, Shaw Towers, Singapore 0718.

**Second Int'l Workshop on Advances in Robot Kinematics:** Sept. 10-12, 1990, Linz, Austria. Sponsors: Research Inst. for Symbolic Computation et al. Submit paper by **Mar. 1, 1990,** to Sabine Stifler, RISC, Johannes Kepler Univ., A-4040 Linz, Austria, phone 43 (7236) 3231-50; or Jadran Lenarcic, Josef Stefan Inst., Univ. of Edvard Kardelj, Jamova 39, 61111 Ljubljana, Yugoslavia, phone 38 (61) 214-399.

***IEEE Trans. on Knowledge and Data Engineering*** plans a special section on enabling technology for knowledge-based systems. Submit paper by **Mar. 2, 1990,** to Howard E. Shrobe, Symbolics, Inc., 8 New England Executive Park, East, Burlington, MA 01803, phone (617) 221-1304; or Se June Hong, IBM T.J. Watson Research Center, PO Box 218, Yorktown Heights, NY 10598, phone (914) 945-2265.

**SIGComm 90 Conf.:** Aug. 1-5, 1990, Philadelphia. Sponsor: ACM SIGComm. Submit paper by **Mar. 2, 1990,** to Phil Karn, Bell Communications Research, MS 2P-357, 445 South St., PO Box 1910, Morristown, NJ 07962-1910, phone (201) 829-4299.

**Frontiers 90, Third Symp. on Frontiers of Massively Parallel Computation:** Oct. 8-10, 1990, College Park, Md. Cosponsor: NASA Goddard Space Flight Center. Submit extended abstract by **Mar. 15, 1990,** to Joseph JaJa, Frontiers 90, UMIACS, Univ. of Maryland, A.V. Williams Bldg., College Park, MD 20742, phone (301) 454-1808.

**1990 Int'l Electronics Packaging Conf.:** Sept. 9-13, 1990, Marlborough, Mass. Sponsor: Int'l Electronics Packaging Society. Submit abstract by **Mar. 30, 1990,** to IEPS 1990 Program Committee, 114 N. Hale St., Wheaton, IL 60187, phone (708) 260-1044.

**Second IEEE Symp. on Parallel and Distributed Processing:** Dec. 10-12, 1990, Dallas. Sponsor: Dallas Section of the IEEE Computer Society. Submit paper by **May 1, 1990,** to Behrooz Shirazi, Computer Science and Engineering Dept., Southern Methodist Univ., Dallas, TX 75275, phone (214) 692-2874.

# CALENDAR

In the accompanying Calendar, the IEEE Computer Society logo indicates the conferences the society is sponsoring and participating in; additional conference sponsors are also listed. Other conferences of interest to our readers are included, as well.

For inclusion in Call for Papers or Calendar, submit information **at least six weeks before the month of publication** (i.e., for the **January 1990** issue, send information for receipt by **November 15, 1989**) to Chuck Governale, Calendar Dept., *Computer*, PO Box 3014, Los Alamitos, CA 90720.

## November 1989

**Tencon 89, IEEE Region 10 Conf. on Computer and Communication Systems, Nov. 22-24,** Bombay, India. Cosponsor: IEEE Bombay Section. Contact Kirit J. Sheth, Hakotronics Pvt. Ltd., Victoria Gardens, 20 Sussex Rd., Bombay 400 027, India, phone 91 (22) 872-2888.

**Int'l Workshop on Discrete Algorithms and Complexity, Nov. 20-22,** Fukuoka, Japan. Contact Hiroshi Imai, Computer Science and Communication Engineering Dept., Kyushu Univ. 36, Fukuoka 812, Japan, phone 81 (92) 641-1101.

**First Int'l Conf. on Artificial Intelligence in Industry and Government, Nov. 23-25,** Hyderabad, India. Contact Director, National Centre for Expert Systems, Inst. of Public Enterprise, Osmania Univ. Campus, Hyderabad, 500-007, India.

**Programmable Gate Arrays Symp., Nov. 27,** Toronto, Canada. Sponsor: Information Technology Research Centre. Contact Rosanna Reid, ITEC, Toronto Site Office, 203 College St., Suite 303, Toronto, Ont., M5T 1P9, Canada, phone (416) 978-8558.

**IEEE Workshop on Interpretation of 3D Scenes, Nov. 27-29,** Austin, Texas. Contact Anil K. Jain, Computer Science Dept., Michigan State Univ., A-714 Wells Hall, East Lansing, MI 48824, phone (517) 353-5150.

**Second OSI Product Integration Conf., Nov. 28-Dec. 1,** Washington, DC. Sponsor: Corporation for Open Systems International. Contact Conf. Manager, US Professional Development Inst., 1734 Elton Rd., Suite 221, Silver Spring, MD 20903, phone (301) 445-4400.

## December 1989

**WSC 89, Winter Simulation Conf., Dec. 3-6,** Washington, DC. Cosponsors: Society for Computer Simulation et al. Contact Sallie Sheppard, Office of Associate Provost, 103 Academic Bldg., Texas A&M Univ., College Station, TX 77843, phone (409) 845-3210; or Philip Heidelberger, IBM Research Div., T.J. Watson Research Center, Hawthorne, PO Box 704, Yorktown Heights, NY 10598, phone (914) 789-7156.

**First Caribbean Conf. on Artificial Intelligence, Dec. 4-5,** St. Augustine, Trinidad. Sponsor: Univ. of the West Indies Faculty of Engineering. Contact Myron Chin, Faculty of Engineering, Univ. of the West Indies, St. Augustine, Trinidad, West Indies, phone (809) 663-2222.

**First Int'l Conf. on Deductive and Object-Oriented Databases, Dec. 4-6,** Kyoto, Japan. Sponsor: Information Processing Society of Japan. Contact Won Kim, MCC, 3500 W. Balcones Center Dr., Austin, TX 78759, phone (512) 338-3439; Jean-Marie Nicholas, ECRC Arabellastr. 17, 8000 Munich 81, FRG, phone 49 (89) 926-99-110; or Shojiro Nishio, Information and Computer Science Dept., Faculty of Engineering Sciences, Osaka Univ., Toyonaka, Osaka, 560 Japan, phone 81 (6) 853-5737.

**Fifth Computer Security Applications Conf., Dec. 4-8,** Tucson, Ariz. Cosponsors: American Society for Industrial Security, Aerospace Computer Security Associates. Contact Marshall D. Abrams, Mitre Corp., 7525 Colshire Dr., MS Z506, McLean, VA 22102, phone (703) 883-6938.

**10th Real-Time Systems Symp., Dec. 5-7,** Santa Monica, Calif. Contact Al Mok, Computer Science Dept., TAY 3-140C, Univ. of Texas, Austin, TX 78712, phone (512) 471-9542.

**SIGSoft 89, Third Testing, Analysis, and Verification Symp., Dec. 6-8,** Key West, Fla. Cosponsor: ACM. Contact Richard A. DeMillo, Purdue Univ., Computer Science Dept., West Lafayette, IN 47907, phone (317) 494-7823.

**Government Communications Conf., Dec. 6-8,** Washington, DC. Cosponsors: Corporation for Open Systems et al. Contact US Professional Development Inst., 1734 Elton Rd., Suite 221, Silver Spring, MD 20903, phone (301) 445-4400.

**Second Int'l Conf. on Formal Description Techniques/Distributed Systems, Dec. 6-9,** Vancouver, B.C., Canada. Cosponsors: ACM, Univ. of British Columbia. Contact Son T. Vuong, Univ. of British Columbia, 6356 Agricultural Rd., Vancouver, B.C., Canada, phone (604) 228-6366.

**Hi Tech Update 89, Dec. 7,** Ottawa, Ont., Canada. Sponsor: Carleton Univ. Faculty of Engineering. Contact Conf. Coll, Inc., 1138 Sherman Dr., Ottawa, Ont., Canada K2C 2M4, phone (613) 224-1741.

**Third Int'l Workshop on Petri Nets and Performance Models, Dec. 11-13,** Kyoto, Japan. Cosponsors: Society of Instrument and Control Engineers et al. Contact Shojiro Nishio, Information and Computer Science Dept., Faculty of Engineering Sciences, Osaka Univ., Toyonaka, Osaka, 560 Japan, phone 81 (6) 853-5737.

**Workshop on Heterogenous Database Systems, Dec. 11-13,** Evanston, Ill. Cosponsor: National Science Foundation. Contact Peter Scheuermann, Electrical Engineering and Computer Science Dept., Technical Inst., Northwestern Univ., Evanston, IL 60201, phone (312) 491-7141.

**Fourth SIAM Conf. on Parallel Processing for Scientific Computing, Dec. 11-13,** Chicago. Sponsor: Society for Industrial and Applied Mathematics. Contact SIAM Conf. Coordinator, 117 S. 17th St., 14th Floor, Philadelphia, PA 19103-5052, phone (215) 564-2929.

**KBCS 89, Conf. on Knowledge-Based Computer Systems: Dec. 11-13,** Bombay. Sponsor: Government of India Dept. of Electronics. Contact S. Ramani, KBCS 89, National Centre for Software Technology, Gulmohar Cross Rd. No. 9, Juhu, Bombay 400 049, India.

**Second Nat'l Conf. on Computer Security Awareness and Practices, Dec. 12-14,** Washington, DC. Sponsor: *Government Computer News*. Contact US Professional Development Inst., 1734 Elton Rd., Suite 221, Silver Spring, MD 20903, phone (301) 445-4400.

**21st Nat'l EDI Systems Conf., Dec. 12-14,** Washington, DC. Sponsor: Electronic Data Interchange Association. Contact EDIA, 225 Reinekers Lane, Suite 550, Alexandria, VA 22314, phone (703) 838-8042.

**EuroComm, Int'l Telecommunications Congress, Dec. 12-15,** Amsterdam, The Netherlands. Contact Europaplein, 1078 GZ Amsterdam, phone 31 (20) 549-1212.

**Int'l Conf. on CAD/CAM and Advanced Manufacturing Technology in Israel, Dec. 19-21,** Jerusalem, Israel. Cosponsors: Israel Society for CAD/CAM, SME. Contact Lawrence R. Odess, Ortra, PO Box 50432, 61500 Tel Aviv, Israel, phone 972 (3) 971-3991 or 664-825.

**Ninth Conf. on Foundations of Software Technology and Theoretical Computer Science, Dec. 19-21,** Bangalore, India. Contact C.E. Veni Madhavan, Tata Research Development and Design Center, 1 Mangaldas Rd., Pune 411001, India, phone (212) 662-453.

**Sixth Israeli Conf. on Artificial Intelligence and Computer Vision, Dec. 26-27,** Tel Aviv. Sponsor: Information Processing Assoc. of Israel. Contact IPA, PO Box 13009, 91130 Jerusalem, Israel.

## January 1990

**HICSS 23, 23rd Hawaii Int'l Conf. on System Sciences, Jan. 3-5,** Kailua-Kona, Hawaii. Sponsor: Univ. of Hawaii. Contact Luqi, Computer Science Dept., Naval Postgraduate School, Monterey, CA 93943, phone (408) 646-2735.

**First Int'l Symp. on Artificial Intelligence and Mathematics, Jan. 3-5,** Fort Lauderdale, Fla. Contact Frederick Hoffman, Mathematics Dept., Florida Atlantic Univ., PO Box 3091, Boca Raton, FL 33431-0991, phone (407) 367-3340.

**Supercomputing Europe 90, Jan. 10-12,** London. Sponsors: Univ. of London Computer Centre et al. Contact Gerry Parker, Meridien Pacific Group, 116 E. Blitdale Ave., Suite 2, Mill Valley, CA 94941, phone (415) 381-2256.

**OE LASE 90, Optics, Electro-Optics, and Laser Applications in Science and Engineering, Jan. 14-19,** Los Angeles. Sponsor: SPIE. Contact Int'l Society for Optical Engineering, PO Box 10, Bellingham, WA 98227-0010.

**IJCNN 90, Int'l Joint Conf. on Neural Networks, Jan. 15-19,** Washington, DC. Cosponsors: IEEE, INNS. Contact Deverman and Assoc., 4233 Spring St., No. 99, La Mesa, CA 92041, phone (619) 462-6800.

**POPL 90, 17th Symp. on Principles of Programming Languages, Jan. 17-19,** San Francisco. Sponsors: ACM SIGAct, SIGPlan. Contact Assoc. for Computing Machinery, 11 W. 42nd St., New York, NY 10036, phone (212) 869-7440.

**IEEE Design Automation Workshop, Jan. 21-24,** Scottsdale, Ariz. Contact Paul Drongowski, Computer Engineering and Science Dept., Case Western Reserve Univ., Cleveland, OH 44106, phone (216) 368-5028.

**Winter 1990 Usenix Tech. Conf., Jan. 22-26,** Washington, DC. Contact Daniel V. Klein, Software Engineering Inst., Carnegie Mellon Univ., Pittsburgh, PA 15213-3890, phone (412) 268-7791.

**Second IEEE Int'l Conf. on Wafer Scale Integration, Jan. 23-25,** San Francisco. Contact Joe Brewer, 351 White Cedar Ln., Severna Park, MD 21146, phone (301) 765-1247.

**Ninth Int'l Conf. on Computing Methods In Applied Sciences and Engineering, Jan. 29-Feb. 2,** Paris. Cosponsor: INRIA. Contact INRIA, Service des Relations Exterieures, Domaine de Coloques—BP 105, 78153, Rocquencourt, France; phone 33 (1) 39-63-5600.

## February 1990

**1990 IEEE Aerospace Applications Conf., Feb. 3-10,** Vail, Colo. Sponsor: IEEE South Bay Harbor Section. Contact Douglas Theis, Aerospace Corp., M6/204, PO Box 92957, Los Angeles, CA 90009.

**First Workshop on Neural Networks: Academic/Industrial/NASA/Defense Technical Interchange and Tutorials, Feb. 5-6,** Auburn, Ala. Sponsors: NASA/Center for Commercial Development of Space Power and Advanced Electronics et al. Contact Mary Lou Padgett, John Wu, or T. Roppel, EE Dept., 200 Broun Hall, Auburn Univ., AL 36849, phone (205) 844-1855.

**Sixth Int'l Conf. on Data Engineering, Feb. 5-9,** Los Angeles. Contact Joseph E. Urban, Arizona State Univ., College of Engineering and Applied Sciences, Computer Science Dept., Tempe, AZ 85287, phone (602) 965-2774; or Sixth Int'l Conf. of Data Engineering, IEEE Computer Society, 1730 Massachusetts Ave. NW, Washington, DC 20036-1903, phone (202) 371-1013.

**Applications Technology Conf., Feb. 12-15,** San Jose, Calif. Sponsor: American Electronics Assoc. Contact Ed Teja, American Electronics Assoc., 5201 Great American Pkwy., Santa Clara, CA 95054, phone (503) 231-9914.

**Eurasip Workshop on Neural Networks, Feb. 15-17,** Sesimbra, Portugal. Cosponsors: European Assoc. for Signal Processing, IEEE, Instituto de Engenharia de Sistemas e Computadores. Contact Luis B. Almeida, INESC, Apartado 10105, P-1017 Lisboa Codex, Portugal, phone 351 (1) 544-607.

**Ninth IEEE Computer Fair, Feb. 16-17,** Huntsville, Ala. Cosponsors: IEEE Computer Society Huntsville Section, IEEE

Huntsville Section. Contact Terrence A. Mizell, 418 Isbell Rd., Hazel Green, AL 35750, phone (205) 828-0803

**1990 Workshop on VLSI, Feb. 18-21,** Clearwater Beach, Fla. Contact Sami Al-Arian, Computer Science and Engineering Dept., Univ. of South Florida, Tampa, FL 33620, phone (813) 974-3544.

**CSC 90, 18th Computer Science Conf., Feb. 20-22,** Washington, DC. Sponsor: ACM. Contact Barbara Kyriakakis, Computer Science Dept., George Mason Univ., Fairfax, VA 22030, phone (703) 323-2318.

**IEEE Computer Society Compcon Spring 90, Feb. 26-Mar. 2,** San Francisco. Contact Kenichi Miura, Computational Research Dept., MS B2-7, Fujitsu America, 3055 Orchard Dr., San Jose, CA 95134-2017, phone (408) 432-1300, ext. 5408 or 5723; or Compcon Spring 90, IEEE Computer Society, 1730 Massachusetts Ave. NW, Washington, DC 20036-1903, phone (202) 371-1013.

**Nepcon West 90, Nat'l Electronic Packaging and Production Conf., Feb. 26-Mar. 1,** Anaheim, Calif. Contact Michael Critser, Nepcon Conf. Group, 1350 E. Touhy Ave., Des Plaines, IL 60017-5060, phone (312) 299-9311.

**Third Int'l Software for Strategic Systems Conf., Feb. 27-28,** Huntsville, Ala. Cosponsors: IEEE Computer Society Huntsville Chapter et al. Contact Continuing Education Div., Univ. of Alabama in Huntsville, Tom Bevill Center 285, Huntsville, AL 35899, phone (800) 448-4035 or (205) 895-6372.

## March 1990

**Eighth Nat'l Conf. on Ada Technology, Mar. 5-8,** Atlanta. Contact Eighth Nat'l Conf. of Ada Technology, US Army Communications—Electronics Command, Attn.: AMSEL-RD-SE-CRM (Kay Trezza), Fort Monmouth, NY 07703-5000.

**CAIA 90, Sixth IEEE Conf. on Artificial Intelligence Applications, Mar. 5-9,** Santa Barbara, Calif. Contact CAIA 90, IEEE Computer Society, 1730 Massachusetts Ave. NW, Washington, DC 20036-1903, phone (202) 371-1013; or Se June Hong, IBM T.J. Watson Research Center, Rm. 31-206, PO Box 218, Yorktown Heights, NY 10598, phone (914) 945-2265.

**Int'l Conf. on Neural Networks, Mar. 6-8,** Lyon, France. Sponsors: Associazione Italiana per l'Informatica ed Il Calcolo Automatico et al. Contact Solange Dubeauclard, 1030 N. Glenhurst, Birmingham, MI 48009, phone (313) 647-7833.

**Parbase 90, Int'l Conf. on Databases, Parallel Architectures, and Their Applications, Mar. 6-9,** Miami Beach. Sponsor: Florida Int'l Univ. Contact Parbase 90, School of Computer Science, Florida Int'l Univ., Miami, FL 33199, phone (305) 554-3386 or 3429.

**EDAC 90, European Design Automation Conf., Mar. 12-15,** Glasgow, Scotland. Contact Gordon Adshead, CEP Consultants, 26-28 Albany St., Edinburgh, EH1 3QH, Scotland, UK, phone 44 (31) 557-2478.

**IEEE Computer Society 1990 Int'l Conf. on Computer Languages, Mar. 12-16,** New Orleans. Contact Boumediene Belkhouche, Computer Science Dept., Tulane Univ., PO Box 5079, 301 Stanley Thomas Hall, New Orleans, LA 70118, phone (504) 865-5840.

**NCGA 90, Mar. 19-22,** Anaheim, Calif. Contact NCGA, 2722 Merrilee Dr., Suite 200, Fairfax, VA 22031, phone (703) 698-9600.

**IPCCC, Ninth IEEE Int'l Phoenix Conf. on Computers and Communications, Mar. 21-23,** Scottsdale, Ariz. Cosponsor: IEEE Communications Society. Contact Forouzan Golshani, Computer Science Dept., Arizona State Univ., Tempe, AZ 85287, phone (602) 965-2855.

**Eighth Built-In Self Test Workshop, Mar. 21-23,** Charleston, S.C. Sponsors: IEEE Test Technology Committee, IEEE International Test Conf. Contact Richard Sedmak, Self-Test Services, 6 Lindenwold Terr., Ambler, PA 19002, phone (215) 628-9700.

**1990 Symp. on Interactive 3D Graphics, Mar. 25-28,** Snowbird, Utah. Sponsors: US Office of Naval Research et al. Contact Richard Riesenfeld, Univ. of Utah, Computer Science Dept., 3190 Merrill Engineering Bldg., Salt Lake City, Utah 84112, phone (801) 581-8224.

**Conf. on AI, Simulation, and Planning in High-Autonomy Systems, Mar. 26-27,** Tucson, Ariz. Cosponsors: Univ. of Arizona et al. Contact B. Zeigler, Electrical and Computer Engineering Dept. Office of Engineering Professional Development, Univ. of Arizona, Box 9 Harvill Bldg., Tucson, AZ 85721, phone (602) 621-3054 or (602) 743-9551.

**ICSE 12, 12th Int'l Conf. on Software Engineering, Mar. 26-30,** Nice, France. Cosponsors: ACM, AFCET. Contact Francois-Regis Valette, CERT/DERI, PO Box 4026-2, Ave. Edouard Belin-31055 Toulouse, France, phone (33) 61-55-71-11; ICSE 12, AFCET, 156 Bd. Pereire, 75017 Paris, France; or IEEE Computer Society, 1730 Massachusetts Ave. NW, Washington, DC 20036-1903, phone (202) 371-1013.

**1990 Int'l Conf. on Extending Database Technology, Mar. 26-30,** Venice, Italy. Cosponsors: EDBT Foundation et al. Contact Michael L. Brodie, Intelligent Database Systems Dept., GTE Labs, 40 Sylvan Rd., MS 62, Waltham, MA 02254, phone (617) 466-2256.

**1990 AAAI Spring Symp. on the Theory and Application of Minimal-Length Encoding, Mar. 27-29,** Stanford, Calif. Contact Edwin Pednault, AT&T Bell Laboratories, Rm. 4F-611, Crawfords Corner Rd., Holmdel, NJ 07733, phone (201) 949-1074.

## April 1990

**CHI 90, Human Factors in Computing Systems 1990, Apr. 1-5,** Seattle. Sponsor: ACM. Contact Assoc. for Computing Machinery, 11 W. 42nd St., New York, NY 10036.

**Fourth Parallel Processing Symp., Apr. 3-5,** Fullerton, Calif. Cosponsor: California State Univ. at Fullerton. Contact Larry H. Canter, c/o Computer Systems Approach, 1140 S. Raymond Ave., Suite B., Fullerton, CA 92631, phone (714) 738-3414.

**Flairs 90, Florida AI Research Symp., Apr. 3-6,** Cocoa Beach, Fla. Contact Avelino J. Gonzalez, Computer Engineering Dept., Univ. of Central Florida, Orlando, FL 32816, phone (407) 281-5027.

**1990 Symp. on Applied Computing, Apr. 5-6,** Fayetteville, Ark. Cosponsors: Univ. of Arkansas, UA Student ACM Chapter. Contact Hal Berghel, Univ. of Arkansas, Computer Science Dept., Fayetteville, AR 72701, phone (501) 575-7343.

**Int'l Topical Meeting on Optical Computing, Apr. 8-12,** Kobe, Japan. Cosponsors: SPIE et al. Contact S. Ishihara, Business Center for Academic Societies Japan, 3-23-1, Hongo, Bunkyo-ku, Tokyo 113, Japan, phone 81 (3) 817-5831.

**1990 IEEE VLSI Test Workshop, Apr. 10-11,** Atlantic City, NJ. Cosponsor: IEEE Philadelphia Section. Contact Wesley E. Radcliffe, IBM East Fishkill, Dept. 277, Bldg. 321-5E1, Hopewell Junction, NY 12533, phone (914) 894-4346.

**Disco 90, Int'l Symp. on Design and Implementation of Symbolic Computation Systems, Apr. 10-12,** Capri, Italy. Contact Alfonso Miola, Dip. Informatica e Sistemistica, Via Buonarroti, 12, 00185 Roma, Italy, phone 39 (6) 731-2367.

**Applications of Artificial Intelligence VIII, Apr. 15-18,** Orlando, Fla. Sponsor: SPIE. Contact Mohan M. Trivedi, Univ. of Tennessee, Electrical and Computer Engineering, Ferris Hall, Knoxville, TN 37996-2100, phone (615) 974-5450.

**13th IEEE Workshop on Design for Testability, Apr. 17-20,** Vail, Colo. Contact T.W. Williams, IBM, PO Box 1900, Dept. 67A/021B, Boulder, CO 80301-9191, phone (303) 924-7692.

**First Int'l Conf. on Systems Integration, Apr. 23-26,** Morristown, N.J. Sponsor: New Jersey Inst. of Technology. Contact Peter A. Ng, Computer and Information Science Dept., New Jersey Inst. of Technology, Newark, NJ 07102, phone (201) 596-3387.

**COIS 90, Conf. on Office Information Systems, Apr. 25-27,** Cambridge, Mass. Sponsor: ACM. Contact Robert B. Allen, Rm. 2A-367, Bellcore, 444 South St., Morristown, NJ 07960-1910, phone (201) 829-4280, 4315.

**First Int'l Symp. on Environments and Tools for Ada, Apr. 30-May 2,** Redondo Beach, Calif. Cosponsor: ACM. Contact Stowe Boyd, Meridian Software Systems, 23141 Verdugo Dr., Suite 105, Laguna Hills, CA 92653, phone (714) 727-0700, ext. 222; or Dewayne E. Perry, AT&T Bell Laboratories, 600 Mountain Ave., Murray Hill, NJ 07974, phone (201) 582-2529.

## May 1990

**IAAI 90, Second Conf. on Innovative Applications of Artificial Intelligence, May 1-3,** Washington, DC. Sponsor: American Assoc. for Artificial Intelligence. Contact AAAI, 445 Burgess Dr., Menlo Park, CA 94025, phone (415) 328-3123.

**21st Pittsburgh Conf. on Modeling and Simulation, May 3-4,** Pittsburgh. Sponsors: Univ. of Pittsburgh et al. Contact William G. Vogt or Marlin H. Mickle, Modeling and Simulation Conf., 348 Benedum Engineering Hall, Univ. of Pittsburgh, Pittsburgh, PA 15261.

**10th IEEE Symp. on Mass Storage Systems, May 6-10,** Monterey, Calif. Contact Bernard T. O'Lear, NCAR, PO Box 3000, Boulder, CO 80307, phone (303) 497-1268.

**CompEuro 90, IEEE Int'l Conf. on Computer Systems and Software Engineering, May 7-9,** Tel Aviv. Cosponsors: IEEE Region 8, IEEE Israel Section, IEEE Computer Society Israel Chapter. Contact CompEuro 90 Conf. Secretariat, c/o ORTRA, 2 Kaufman St., PO Box 50432, Tel Aviv, 61500, Israel, phone 972 (3) 664-825.

**1990 IEEE Symp. on Research in Security and Privacy, May 7-9,** Oakland, Calif. Contact Deborah Cooper, Unisys, 5731 Slauson Ave., Culver City, CA 90230, phone (213) 338-3727.

**Fourth Int'l Symp. on Knowledge Engineering, May 7-11,** Barcelona, Spain. Sponsor: Madrid Polytechnic Univ. Contact Jose R. Chelala, ISKE, Alvarez de Baena, 3-2, 28006 Madrid, Spain.

**1990 SID Int'l Symp., May 14-18,** Las Vegas. Contact Howard L. Funk, IBM Corp., 10/641 3B-60, Old Orchard Rd.,Armonk, NY 10504, phone (914) 765-6409.

**43rd SPSE Conf., May 20-25,** Rochester, N.Y. Sponsor: Society for Imaging Science and Technology. Contact Michael M. Shahin, Xerox Corp., Webster Research Center, 800 Phillips Rd., 0114-38D, Webster, NY 14580, phone (716) 422-2011.

**First Conf. on Visualization in Biomedical Computing,** May 22-25, Atlanta. Cosponsors: Nat'l Science Foundation et al. Contact Norberto Ezguerra, Bioengineering Center, Georgia Tech, Atlanta, GA 30332, phone (404) 894-7026 or 3964.

**SIGMetrics 90, May 22-25,** Boulder, Colo. Sponsor: ACM. Contact Gary J. Nutt, Univ. of Colorado, Boulder, CO 80301; or Herb Schwetman, MCC, 3500 W. Balcones Center Dr., Austin, TX 78759, phone (512) 338-3428.

**20th Int'l Symp. on Multiple-Valued Logic, May 23-25,** Charlotte, N.C. Contact George Epstein, Computer Science Dept., Univ. of North Carolina at Charlotte, 214 Kennedy Bldg., Charlotte, NC 28223, phone (704) 547-4566; or Carolyn F. Blalock, Office of Continuing Education, Univ. of North Carolina at Charlotte, Charlotte, NC 28223, phone (704) 547-4861.

**ICCI 90, Int'l Conf. on Computing and Information, May 23-26,** Niagara Falls, Canada. Sponsor: Natural Sciences and Engineering Research Council of Canada. Contact Waldemar W. Koczkodaj, ICCI 90, Laurentian Univ., CoSc, Sudbury, Ont., Canada P3E 2C6.

**1990 American Control Conf., May 23-25,** San Diego, Calif. Sponsor: American Automatic Control Council. Contact Dagfinn Gangsaas, Boeing Advanced Systems, PO Box 3707, MS 33-12, Seattle, WA 98124-2207, phone (206) 241-4348.

**17th Int'l Symp. on Computer Architecture, May 28-31,** Seattle. Cosponsor: ACM. Contact Jean L. Baer or Larry Snyder, Univ. of Washington, Computer Science Dept., FR-35, Seattle, WA 98195, phone (206) 543-1695.

**ICDCS 10, 10th Int'l Conf. on Distributed Computing Systems, May 28-June 1,** Paris. Cosponsor: INRIA. Contact R. Popescu-Zeletin, GMD-FOKUS, Hardenbergplatz 2, D-1000 Berlin 12, West Germany, phone 49 (30) 25499-206; Jack Stankovic, Computer and Information Science Dept., Univ. of Massachusetts, Amherst, MA 01003, phone (413) 545-0720; or ICDCS 10, IEEE Computer Society, 1730 Massachusetts Ave. NW, Washington, DC 20036-1903, phone (202) 371-1013.

**11th Conf. of the Canadian Applied Mathematics Society, May 29-June 1,** Halifax, N.S., Canada. Cosponsors: CAMS et al. Contact Mary Meidell, Continuing Education Dept., Technical Univ. of Nova Scotia, PO Box 1000, Halifax, NS B3J 2X4, Canada, phone (902) 429-8300, ext. 2420.

## June 1990

**CBMS 90, Third IEEE Symp. on Computer-Based Medical Systems, June 3-6,** Chapel Hill, N.C. Cosponsor: IEEE Engineering in Medicine and Biology Society. Contact James N. Brown, Jr., Research Triangle Inst., Box 12194, Research Triangle Park, NC 27709, phone (919) 541-6994.

**IEEE Infocom 90, Ninth Conf. on Computer Communications, June 3-7,** San Francisco. Cosponsor: IEEE Communications Society. Contact Infocom 90, IEEE Computer Society, 1730 Massachusetts Ave. NW, Washington, DC 20036-1903, phone (202) 371-1013.

**Int'l Workshop on Rapid System Prototyping, June 5-7,** Triangle Research Park, N.C. Contact Kenneth Anderson, Siemens Corporate Research, 755 College Rd. East, Princeton, NJ 08540, phone (609) 734-6550.

**Eurographics Workshop on Object-Oriented Graphics, June 6-8,** Konigswinter, Federal Republic of Germany. Sponsors: Eurographics and German Society for Informatics. Contact Marja Hegt, O-O Graphics Workshop, CWI, Kruislaan 413, 1098 SJ Amsterdam, The Netherlands, phone 31 (20) 592-4058.

**ACL 90, 28th Conf. of the Assoc. for Computational Linguistics, June 6-9,** Pittsburgh. Contact Don Walker, Bellcore, MRE 2A379, 445 South St., Box 1910, Morristown, NJ 07960-1910, phone (201) 829-4312.

**1990 European Simulation Multiconference, June 10-13,** Erlangen, Federal Republic of Germany. Sponsor: SCS Int'l. Contact Bernd Schmidt, Univ. Erlangen, Computer Science Dept., D-8520, Erlangen, FRG, phone (49) 9131-857-278.

**IFIP Workshop on Design and Test of ASICs, June 11-12,** Hiroshima, Japan. Cosponsors: IPSJ et al. Contact Kozo Kinoshita, Hiroshima Univ., 1-1-80 Higashisendacho, Naka-ku, Hiroshima-shi 730, Japan, phone 81 (87) 249-9150.

**19th Mumps Users' Group Meeting, June 11-15,** Orlando, Fla. Contact Mumps Users' Group, 4321 Hartwick Rd., Suite 100, College Park, MD 20740, phone (301) 779-6555.

**Ninth Int'l Conf. on Analysis and Optimization of Systems, June 12-15,** Antibes, France. Sponsor: INRIA. Contact Conf. Secretariat, INRIA, Service des Relations Exterieures, Domaine de Voluceau—BP 105, 78153 Le Chesnay Cedex, France, phone 33 (1)-39-63-5500.

**IAPR Workshop on Syntactic and Structural Pattern Recognition, June 13-15,** Murray Hill, N.J. Sponsor: Int'l Assoc. for Pattern Recognition. Contact Henry S. Baird, AT&T Bell Laboratories, Rm. 2C-557, 600 Mountain Ave., Murray Hill, NJ 07974, phone (201) 582-5744.

**Third Int'l Symp. on Image Conservation, June 17-20,** Rochester, N.Y. Sponsor: Society for Imaging Science and Technology. Contact Charlton Bard, 74 Cornwall Lane, Rochester, NY 14617, phone (716) 342-3174.

**10th Int'l Conf. on Pattern Recognition, June 17-21,** Atlantic City, NJ. Contact Herbert Freeman, CAIP Center, 605 Hill, Rutgers Univ., New Brunswick, NJ 08903, phone (201) 932-4208.

**IMSC 90, Int'l Mobile Satellite Conf., June 18-20,** Ottawa, Canada. Cosponsors: NASA, Canadian Dept. of Communications. Contact IMSC 90 Organizing Committee, c/o D. Hugh

M. Reekie, Dept. of Communications, 300 Slater St., Ottawa, Ont., Canada, K1A 0C8.

**Seventh Int'l Conf. on Testing Computer Software, June 18-21,** San Francisco. Contact Genevieve Houston-Ludlam, ISTC 90, c/o Frontier Technologies, 190 Admiral Cochran Dr., Suite 180, Annapolis, MD 21401, phone (301) 266-8244.

**Second Int'l Conf. on Software Engineering and Knowledge Engineering, June 21-23,** Skokie, Ill. Sponsors: Knowledge Systems Inst., Univ. of Pittsburgh, and Inst. for Information Industries, Taiwan. Contact Shi-Kuo Chang, Computer Science Dept., Univ. of Pittsburgh, 322 Alumni Hall, Pittsburgh, PA 15260, phone (412) 624-8490.

**NECC 90, 11th Nat'l Educational Computing Conf., June 25-27,** Nashville, Tenn. Sponsor: Int'l Council for Computers in Education. Contact John D. McGregor, Computer Studies Dept., Murray State Univ., Murray, KY 42071, phone (502) 762-2614.

**DAC 90, 27th ACM/IEEE Design Automation Conf., June 25-29,** Orlando, Fla. Contact Pat Pistilli, MP Associates, 7490 Clubhouse Rd., Suite 102, Boulder, CO 80301, phone (303) 530-4333.

**Int'l Symp. on Fuzzy Approach to Reasoning and Decision Making, June 25-29,** Bochyne, Czechoslovakia. Sponsor: Int'l Fuzzy System Assoc. Contact Vilem Novak, Minin Inst., Czechoslovakia Academy of Sciences, A. Rimana 1768, 70800 Ostrava-Poruba, Czechoslovakia.

**Advanced Research Workshop on 3D Imaging in Medicine, June 25-29,** Travemuende, Federal Republic of Germany. Sponsor: NATO. Contact Linda Houseman, Computer Science Dept., Univ. of North Carolina, Box 3175, Sitterson Hall, Chapel Hill, NC 27599, phone (919) 962-1758 (for the Americas); or Andreas Pommert, Inst. f[a..]ur Mathematik und Datenverarbeitung in der Medizin, Univ. Krankenhaus Eppendorf, Martinistrasse 52, 2000 Hamburg 20, Federal Republic of Germany, phone 49 (40) 468-2300 (for Europe, Asia, Australia, and Africa).

**EKAW 90, Fourth European Knowledge Acquisition for Knowledge-Based Systems Workshop, June 25-29,** Amsterdam. Contact John H. Boose, Advanced Technology Center, Boeing Computer Services 7L-64, PO Box 24346, Seattle, WA 98124, phone (206) 865-3253.

**FTCS 20, 20th Int'l Symp. on Fault Tolerant Computing, June 26-28,** Newcastle upon Tyne, England. Cosponsors: Centre for Software Reliability, British Computer Society, IEE. Contact Neil Speirs, Computing Lab, Univ. of Newcastle upon Tyne, Newcastle upon Tyne, NE1 7RU, UK, phone 44 (91) 232-8511.

**Compass 90, Fifth Conf. on Computer Assurance: Systems Integrity, Software Safety, and Process Security, June 26-29,** Gaithersburg, Md. Cosponsors: IEEE Aerospace and Electronics Society, IEEE National Capital Area Council. Contact Dolores Wallace, National Inst. of Standards and Technology, Gaithersburg, MD 20899; (301) 975-3340.

**CGI 90, Computer Graphics Int'l 1990, June 26-30,** Kent Ridge, Singapore. Sponsors: Computer Graphics Society, Inst. of Systems Science, Singapore. Contact Juzar Motiwalla, CGI 90, ISS, Nat'l Univ. of Singapore, Kent Ridge, Singapore 0511, phone (65) 772-2075.

## July 1990

**Roundtable Discussion on Vision-Based Vehicle Guidance, July 2,** Tokyo. Sponsor: Committee of IEEE Int'l Workshop on Intelligent Robots and Systems. Contact Ichiro Masaki, Computer Science Dept., GM Research Labs, 30500 Mound Rd., Warren, MI 48090-9055, phone (313) 986-1466.

**Second Int'l Symp. on Databases in Parallel and Distributed Systems, July 2-4,** Dublin, Ireland. Cosponsor: ACM. Contact Rakesh Agrawal, AT&T Bell Labs, Rm. 3D450, 600 Mountain Ave., Murray Hill, NJ 07974, phone (201) 582-2250; or David Bell, Inst. of Informatics, Univ. of Ulster, Jordanstown, County Antrim, Northern Ireland BT370QB, phone (0232) 365-131.

**Second Int'l Conf. on Economics and Artificial Intelligence, July 2-6,** Paris. Sponsor: AFCET. Contact J-L. Le Moigne, GRASCE, Univ. Aix Marseille III, 3, ave. Robert Schuman, 13628, Aix en Provence, France; or P. Bourgine, 26, rue St. Louis, 78000, Versailles, France.

**Iberamia 90, Second Ibero-American Conf. on AI, July 9-13,** Morelia, Michoacan, Mexico. Sponsors: Centro Regional de Ensenanza en Informatica (Spain) et al. Contact Iberamia 90, Atn. Srita. Ma. Antonieta Alvarez Perez, Apartado Postal 70302, C.P. 04510, Mexico, D.F.

**Third Int'l Conf. on Industrial and Engineering Applications for AI and Expert Systems, July 15-18,** Charleston, S.C. Cosponsors: ACM et al. Contact Moonis Ali, Univ. of Tennessee Space Inst., MS15, Tullahoma, TN 37388, phone (615) 455-0631.

**1990 Summer Computer Simulation Conf., July 16-18,** Calgary, Alta., Canada. Sponsor: Society for Computer Simulation. Contact SCS, PO Box 17900, San Diego, CA 92117-7900, phone (619) 277-3888.

**ICALP 90, 17th Int'l Colloquium on Automata, Languages, and Programming, July 16-20,** Coventry, England. Sponsor: Int'l Computers, Ltd. Contact Computer Science Dept., Univ. of Warwick, Coventry CV4 7AL, UK, phone 44 (203) 523-194.

**1990 ACM Conf. on Lisp and Functional Programming, June 27-29,** Nice, France. Contact Gillies Kahn, INRIA Sophia — Antipolis, 2004 Route des Lucioles, 06565 Valbonne Cedex, France, phone (33) 93-65-78-01.

**DIAC 90, Directions and Implications of Advanced Computing, July 28,** Boston. Sponsor: Computer Professionals for Social Responsibility. Contact Douglas Schuler, Boeing Computer Services, MS 7L-64, PO 24346, Seattle, WA 98124-0346, phone (206) 865-3226.

**AAAI 90 National Conf. on AI Workshop, July 31-Aug. 3,** Boston. Sponsor: American Assoc. for Artificial Intelligence. Contact Edward Lafferty, AI Center, Mitre, MS A350, Burlington Rd., Bedford, MA 01730, phone (617) 271-2773.

## August 1990

**SIGGraph 90, 17th Conf. on Computer Graphics and Interactive Techniques, Aug. 6-10,** Dallas. Cosponsor: ACM. Contact Assoc. for Computing Machinery, 11 W. 42nd St., New York, NY 10036, phone (212) 869-7440.

**ICPP 90, 19th Int'l Conf. on Parallel Processing, Aug. 13-17,** St. Charles, Ill. Sponsor: Pennsylvania State Univ. Contact Tse-yun Feng, EE East Bldg, Pennsylvania State Univ., University Park, PA 16802, phone (814) 863-1469.

**Int'l Symp. on Algorithms, Aug. 16-18,** Tokyo. Sponsor: IPSJ Special Interest Group on Algorithms. Contact Tetsuo Asano, Osaka Electro-Communication Univ., Hatsu-cho, Neyagawa, Osaka 572, Japan, phone 81 (720) 24-1131.

**UPADI 90, 21th Convention of the Pan American Federation of Engineering Societies, Aug. 19-24,** Washington, DC. Cosponsors: American Assoc. of Engineering Societies, American Society of Civil Engineers. Contact UPADI 90, ASCE, 345 E. 47th St., New York, NY 10017, phone (212) 705-7218.

**Coling 90, 13th Int'l Conf. on Computational Linguistics, Aug. 20-25,** Helsinki, Finland. Contact Hans Karlgren, KVAL, Skeppsbron 26, S-111 30 Stockholm, Sweden, phone 46 (8) 789-6683.

## September 1990

**ISPRS Commission V Symp., Sept. 3-7,** Zurich, Switzerland. Cosponsors: Int'l Society for Photogrammetry and Remote Sensing et al. Contact ISPRS Commission V Symp., Inst. of Geodesy and Photogrammetry, ETH-Hoenggerberg, 8093 Zurich, Switzerland, phone 41 (1) 377-3051.

**13th Int'l ACM/SIGIR Conf. on Research and Development in Information Retrieval, Sept. 5-7,** Brussels. Contact Jean-Luc Vidick, Univ. Libre de Bruxelles, Avenue F.D. Roosevelt, Infodoc, C.P. 142, 1050 Brussels, Belgium.

**1990 Int'l Electronics Packaging Conf., Sept. 9-13,** Marlborough, Mass. Sponsor: Int'l Electronics Packaging Society. Contact IEPS, 114 N. Hale St., Wheaton, IL 60187, phone (708) 260-1044.

**ITC 90, Int'l Test Conf., Sept. 10-12,** Washington, DC. Cosponsor: IEEE Philadelphia Section. Contact ITC, 1201 Sussex Tpk., Suite 101, PO Box 264, Mt. Freedom, NJ 07970, phone (201) 895-5260.

**Conf. on Managing Expert System Programs and Projects, Sept. 10-12,** Washington, DC. Contact Jay Liebowitz, Management Sciences Dept., George Washington Univ., Washington, DC, phone (202) 994-6969.

**Second Int'l Workshop on Advances in Robot Kinematics, Sept. 10-12,** Linz, Austria. Sponsors: Research Inst. for Symbolic Computation et al. Contact Sabine Stifler, RISC, Johannes Kepler Univ., A-4040 Linz, Austria, phone 43 (7236) 3231-50; or Jadran Lenarcic, Josef Stefan Inst., Univ. of Edvard Kardelj, Jamova 39, 61111 Ljubljana, Yugoslavia, phone 38 (61) 214-399.

**ICCD 90, IEEE Int'l Conf. on Computer Design: VLSI in Computers and Processors, Sept. 16-19,** Cambridge, Mass. Contact Edward M. Middlesworth, Hewlett-Packard, Bldg. 25U, PO Box 10350, Palo Alto, CA 94303-0867, phone (415) 857-5485; or ICCD 90, IEEE Computer Society, 1730 Massachusetts Ave. NW, Washington, DC 20036-1903, phone (202) 371-1013.

**Internal Audit Advanced Technology Forum, Sept. 17-19,** Orlando, Fla. Sponsor: Inst. of Internal Auditors. Contact Stephen M. Paroby, Ernst and Young, 787 Seventh Ave., New York, NY 10019, phone (212) 830-6000.

**Electronic Publishing 90, Sept. 18-20,** Gaithersburg, Md. Sponsor: NIST. Contact Peter R. King, Computer Science Dept., Univ. of Manitoba, Winnipeg, Manitoba, Canada R3T 2N2, phone (204) 474-9935.

**ICARCV 90, Int'l Conf. on Automation, Robotics, and Computer Vision, Sept. 18-21,** Singapore. Contact D.P. Mital, ICARCV 90, School of Electrical and Electronic Engineering, Nanyang Technological Inst., Nanyang Avenue, Singapore 2263.

**Tencon 90, IEEE Region 10 Conf. on Computer and Communication Systems, Sept. 24-27,** Hong Kong. Cosponsor: IEEE Hong Kong Section. Contact Y.S. Cheung, Electrical and Electronic Engineering Dept., Univ. of Hong Kong, Pokfulam, Hong Kong.

## October 1990

**OOPSLA 90, Fifth Conf. on Object-Oriented Programming Systems, Languages, and Applications, Oct. 1-5,** Ottawa, Canada. Cosponsor: ACM. Contact Assoc. for Computing Machinery, 11 W. 42nd St., New York, NY 10036, phone (212) 869-7440.

**InfoJapan 90, Int'l Conf. on Information Technology, Oct. 1-5,** Tokyo. Sponsor: IPSJ. Contact Takuma Yamamoto, Fujitsu, 3-14-1 Hiyoshi, Kohoku-ku, Yokohamashi, Japan.

**1990 IEEE Workshop on Visual Languages, Oct. 4-6,** Skokie, Ill. Cosponsors: Univ. of Pittsburgh et al. Contact S.K. Chang, Computer Science Dept., Univ. of Pittsburgh, Pittsburgh, PA 15260.

**Frontiers 90, Third Symp. on Frontiers of Massively Parallel Computation, Oct. 8-10,** College Park, Md. Cosponsor: NASA Goddard Space Flight Center. Contact Johanna Weinstein, Frontiers 90, UMIACS, Univ. of Maryland, A.V. Williams Bldg., College Park, MD 20742, phone (301) 454-1808.

**Fifth Jerusalem Conf. on Information Technology, Oct. 22-25,** Jerusalem Israel. Sponsor: Information Processing Assoc. of Israel. Contact Abraham Peled, IBM T.J. Watson Research Center, PO Box 704, Yorktown Heights, NY 10598.

**CC 90, Third Int'l Workshop on Compiler Compilers, Oct. 22-26,** Schwerin, German Democratic Republic. Sponsors: German Democratic Republic Academy of Sciences Inst. of Informatics and Computing Technique et al. Contact Michael Albinus, CC 90 Organizing Committee, Akademie der Wissenschaften der DDR, Inst. fur Informatik und Rechentechnik, Rudower Chaussee 5, Berlin, DDR - 1199.

**Visualization 90, Oct. 23-26,** San Francisco. Contact Stephen Levine, Wang Labs, MS 012-250, 1 Industrial Ave., Lowell, MA 01851, phone (508) 967-0798.

**First Japanese Knowledge Acquisition for Knowledge-Based Systems Workshop, Oct. 25-26,** Kyoto, Japan, and Oct. 29-31, 1990, Tokyo. Cosponsors: Kansai Inst. of Information Systems et al. Contact John H. Boose, Advanced Technology Center, Boeing Computer Services 7L-64, PO Box 24346, Seattle, WA 98124, phone (206) 865-3253.

**Compsac 90, 14th Int'l Computer Software and Applications Conf., Oct. 31-Nov. 2,** Chicago. Contact Stephen S. Yau, CIS Dept., 801 CSE, Univ. of Florida, Gainesville, FL 32611, phone (904) 335-8006.

## November 1990

**ICCS 90, Int'l Conf. on Communication Systems, Nov. 5-9,** Singapore. Cosponsors: IEEE Singapore Section et al. Contact ICCS 90, c/o Meeting Planners Pte Ltd., 100 Beach Rd. #33-01, Shaw Towers, Singapore 0718.

**ICCC 90, 10th Int'l Conf. on Computer Communication, Nov. 5-9,** New Delhi, India. Sponsor: Int'l Council on Computer Communication. Contact Saroj Chowla or P.P. Gupta, ICCC 90, CMC Ltd., A-5 Ring Rd., South Extension Part I, New Delhi-110049, India, phone 91 (11) 626-807.

**Intelligent Robotic Systems: Design and Applications, Nov. 6-7,** Philadelphia. Sponsor: SPIE. Contact Mohan M. Trivedi, Univ. of Tennessee, Electrical and Computer Engineering, Ferris Hall, Knoxville, TN 37996-2100, phone (615) 974-5450.

**ICCAD 90, IEEE Int'l Conf. on Computer-Aided Design, Nov. 12-15.** Cosponsor: IEEE Circuits and Systems Society. Contact ICCAD 90, IEEE Computer Society, 1730 Massachusetts Ave. NW, Washington, DC 20036-1903, phone (202) 371-1013.

**Supercomputing 90, Nov. 12-16,** New York City. Cosponsor: ACM. Contact Supercomputing 90, IEEE Computer Society, 1730 Massachusetts Ave. NW, Washington, DC 20036-1903, phone (202) 371-1013.

**13th Western Educational Computing Conf. Nov. 15-16,** Irvine, Calif. Sponsor: California Educational Computing Consortium. Contact Oliver Seely, Jr., California State Univ. at Dominguez Hills, Chemistry, 1000 E. Victoria St., Carson, CA 90747.

**Cognitiva 90, Nov. 20-23,** Madrid. Sponsor: AFCET. Contact Cognitiva 90, c/o AFCET, 156 Bd Pereire 75017 Paris, France, phone 33 (01) 47-66-24-19.

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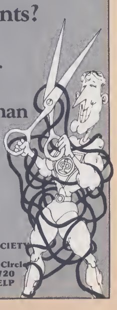

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## NEW JERSEY INSTITUTE OF TECHNOLOGY
### Faculty Positions
### Computer & Information Science

NJIT seeks assistant, associate and full professors for spring/fall 1990. Ph.D. in computer science or closely related field required. Senior level applicants must have proven research and funding record. Positions available in, but not limited to: distributed computing including computer architecture, operating systems, data communications and networking, realtime computing and fault tolerance; software development including compiling, computer graphics, office automation, data management systems, information management systems, cognitive science, and computational linguistics. Department offers B.S., B.A., M.S., and Ph.D., in computer science. Computing facilities include VAX 8800, VAX 8530, IBM 4361, SUN workstations, Symbolics machines, TI Explorers and graphic systems.

NJIT is the technological university of New Jersey with nearly 8,000 students enrolled in Newark College of Engineering, the School of Architecture, College of Science and Liberal Arts, and the School of Industrial Management.

NJIT does not discriminate on the basis of sex, race, color, handicap, religion, national or ethnic origin, or age in employment.

Send resume and name of at least three references to: Personnel Box CIS, New Jersey Institue of Technology, Newark, NJ 07102.

## GEORGE MASON UNIVERSITY
### Faculty Positions in Computer Science

George Mason University is located in Fairfax County, Virginia near the outstanding scientific, cultural, and touristic attractions of Washington, DC. The university has made a major commitment to establish a School of Information Technology and Engineering (SITE) and maintain an outstanding academic and research program in the Department of Computer Science, as well as related research centers in software engineering, artificial intelligence, parallel computation/distributed systems, and computer vision/image processing.

Tenure track and visiting faculty positions are available at all ranks, with the nominal date of appointments commencing September 1990. Candidates for these positions must have an earned doctorate in a relevant field, along with professional accomplishments that are appropriate to the rank sought. They should be interested in both teaching and developing a strong sponsored research program.

The relevant research and teaching areas of interest in Computer Science are: computer communications and networks, software engineering, parallel computation, computer vision/image processing, artificial intelligence, and distributed systems.

Department faculty actively participate in and help support Departmental/School Research Centers in artificial intelligence (R. Michalski, Dir.), parallel computing (P. Wang, Dir.), image processing (A. Sood, Dir.), and software systems engineering (R. Fairley, Dir.).

There are over 90 full-time faculty in SITE, and nearly 25 full-time faculty in Computer Science. There are numerous opportunities for government and industrial interaction in this suburban high technology area, just 15 miles southwest of the Nation's Capital.

For full consideration, please send a detailed resume together with the names of four references, and other supporting material to: Professor Harry Wechsler, Chair, Recruitment Committee, Department of Computer Science, George Mason University, Fairfax, VA 22030, or call at 703-323-2713. Applications are sought by Feb. 1, 1990, and these will receive first priority. AA/EOE.

## School of Engineering
## California Polytechnic State University
## San Luis Obispo, California
### Chairperson,
### Computer Science Department

Applications and nominations are invited for the position of chairperson, Computer Science Department. Position available summer or fall 1990 for a three-year renewable term. Twelve-month appointment, combined instructional and administrative duties; instructional assignment is tenure track. Qualifications required: Ph.D. in computer science or a closely related discipline. Established record of excellence in teaching and applied research suitable for appointment at the rank of Professor. The applicant or nominee must possess management and interpersonal skills appropriate for effective leadership in the department and successful interaction with outside agencies and private industry.

The department is known for excellence in teaching, outstanding bachelor's and master's programs, and successful interaction with government and industry, both in developing sponsored research and in attracting major equipment grants. The computer science program serves 450 undergraduate majors, 75 master's candidates, and over 100 undergraduate majors in computer engineering. Computer facilities for instruction and faculty research are extensive. Cal Poly, a member campus of the California State University, enrolls 15,000 students. The campus is situated on the scenic central coast of California, midway between San Francisco and Los Angeles.

Salary range is $57,156-69,036 plus any authorized general salary increase. Close relations with industry provide opportunities for research and consulting. Deadline: Jan. 15, 1990. Address applications and nominations to:

Dan Stubbs, Chairperson,
Search Committee
Computer Science Department,
School of Engineering
California Polytechnic State University
San Luis Obispo, CA 93407
dstubbs@polyslo.calpoly.edu

Cal Poly is subject to all laws governing affirmative action and equal opportunity employment, including but not limited to Executive Order 11246, Title IX, of the Education Amendment Act and the Rehabilitation Act of 1973. All qualified persons, especially women and minorities, are encouraged to apply. Cal Poly employs only individuals lawfully authorized to work in the United States.

## THE AMERICAN UNIVERSITY IN CAIRO

One Assistant, Associate, or Full Professor needed to teach, in English, undergraduate courses in Computer Science including theory of computing and design of algorithms. Ph.D. required. Rank, salary based on qualifications and experience. Two-year appointment (renewable) beginning September 1990. For expatriates, housing, roundtrip air travel, plus schooling for two children included. Write with curriculum vitae to: Dean George H. Gibson, The American University in Cairo, 866 United Nations Plaza, Suite 517, New York, New York 10017, preferably before December 15.

## UNIVERSITY OF CALIFORNIA, SANTA BARBARA

University of California, Santa Barbara, Electrical and Computer Engineering. Applications are invited for at least four tenure-track faculty positions, available effective 7/1/90, for candidates experienced in image processing/computer vision/speech processing, parallel algorithms, CAD/Solid-State, control systems, and computer engineering. The positions start at the rank of Assistant Professor, although higher level appointments are possible for individuals with outstanding records. Normally completion of a doctorate is required at the time of the appointment. Candidates should have outstanding research potential or a distinguished research reputation, the ability to attract external research funding, and a strong commitment to teaching at the undergraduate and graduate levels. Applicants should send their resumes and the names and addresses of at least four professional references to: Faculty Search Committee, Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106. Applications will be received until the positions are filled. Proof of U.S. Citizenship or eligibility for U.S. employment will be required prior to employment (Immigration Reform and Control Act of 1986). An Equal Opportunity/Affirmative Action employer.

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## SUNY AT BUFFALO

### Department of Computer Science

### Chair

Nominations and applications are invited for the position of Professor and Chair of the Department of Computer Science, to begin Fall 1990.

We seek a distinguished scientist with a prominent research record to lead an expanding department. Candidates should be committed to excellence in research and teaching, be conversant in trends and issues in computer science, and be willing and able to pursue opportunities for strengthening the department. Salary will be extremely competitive, with a flexible research budget.

SUNY-Buffalo is the largest and most comprehensive public university in New York and New England. The department currently has 14 tenured/tenure-track faculty (with plans to increase this number) and 3 lecturers. There are approximately 130 Ph.D. and M.S. students and 200 selectively admitted B.A./B.S. majors. The department is scheduled to move into a new building in Fall 1991. All faculty are actively engaged in research, principally in: AI, parallel algorithms, software quality, systems, and theory, and in interdisciplinary research programs in Advanced Scientific Computing, Cognitive Science, Vision, and with the National Center for Geographic Information and Analysis.

A complete resume, with names of four references, and a description of current research should be sent to: Dr. William J. Rapaport, Computer Science Search Committee, Department of Computer Science, SUNY-Buffalo, Buffalo, NY 14260 (rapaport@cs.buffalo.edu). Application closing date: 1 January 1990 or until position is filled. SUNY-Buffalo is an EO/AA employer.

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## STATE UNIVERSITY OF NEW YORK AT BUFFALO

### Department of Computer Science

### Faculty Positions

Applications are invited for tenure-track faculty positions at all levels, to begin Fall 1990. Applicants for the Assistant Professor level must demonstrate superior research and scholarship potential, and have a Ph.D. in computer science or a related field awarded by September 1, 1990. Applicants for senior positions must have an exceptional record of research achievement.

The University at Buffalo is the most comprehensive public university in New York and New England. The department currently has 14 tenure-track faculty, 3 lecturers and 9 research and adjunct faculty. There are approximately 130 Ph.D. and M.S. students and 200 selectively admitted B.A./B.S. majors. The department is expanding, with additional faculty lines committed annually and a new building under construction. Salaries are extremely competitive.

Primary research areas include: artificial intelligence, computer vision, parallel algorithms, numerical linear algebra, theory of computation, programming languages and performance evaluation. Department members are actively engaged in interdisciplinary research programs in Advanced Scientific Computing, Cognitive Science, Vision, and the NSF National Center for Geographic Information and Analysis. Departmental computing facilities include an Encore multimax, a Vax 11/785, Hypercubes, Sun workstations, Symbolics Lisp Machines, various image processing/graphics systems, micro-based teaching laboratories, and ready access to university-wide computing facilities.

Resumes and names of four references should be directed to: Dr. Deborah Walters, Chair of Search Committee, Department of Computer Science, 226 Bell Hall, SUNY at Buffalo, Buffalo, NY 14260. Net Address: walters@cs.buffalo.eduNFor full consideration applications should be received by January 1, 1990. SUNY is an Equal Opportunity/Affirmative Action employer.

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## UNIVERSITY OF PITTSBURGH

### Tenure Track Position

### Department of Electrical Engineering

The Department of Electrical Engineering has an immediate tenure-track opening in computer engineering. Preferred areas include (but are not limited to) VLSI design, artifical intelligence, computer architecture, and computer vision. All applicants must possess a Ph.D. and must have a strong commitment to teaching and research. Rank and salary are open. The Department has 400 undergraduate students and 180 graduate students enrolled in the M.S. and Ph.D. programs. The University has extensive research and computational facilities, including 4 VAX 8800s and a Cray Y-MP/832 supercomputer. In addition, the Department has its own network of sun workstations. Qualified applicants should send their resume to: Chairman, Search Committee, Department of Electrical Engineering, University of Pittsburgh, Pittsburgh, PA 15261. The University of Pittsburgh is an equal opportunity/affirmative action employer.

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## UNIVERSITY OF CALIFORNIA, SANTA CRUZ

Computer & Information Sciences at UC Santa Cruz invites applications for two positions of Assistant Professor, effective July 1, 1990. One position is in Computer Graphics (#194-890), the other is in Distributed Systems, Operating Systems, and Programming Languages, (#195-890). A Ph.D. in Computer Science or equivalent is required. Candidates must have demonstrated research potential, and will be evaluated on their research record, teaching, professional activities, potential for distinction, and letters of recommendation. Salary range: $44,200-$46,400. Send applications, including curriculum vitae with cover letter, publications and teaching evaluations, and 3 letters of recommendation, promptly to the following address: Chair, Computer Faculty Search Committee, Baskin Center for Computer Engineering & Information Sciences, Applied Sciences Building, University of California, Santa Cruz, CA 95064. Applications must be received by February 1, 1990. If either position remains unfilled, applications received by April 1, 1990, will be considered. Please refer to Position #194-890 or #195-890 in your reply. UCSC is an EEO/AA/IRCA employer.

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## GEORGIA STATE UNIVERSITY

### Computer Information Systems

### Faculty Positions

The Department of Computer Information Systems invites applications for tenure-track faculty positions at the rank of Instructor, Assistant, Associate and Professor in Computer Information Systems. The department currently seeks faculty with strong research and teaching capabilities in the following areas: Software engineering, Telecommunications, database management, computer architecture, operating systems, and data structures, but welcomes applications from other areas as well.

Candidates at the associate/professor level must have a Ph.D. or equivalent. Candidates at the assistant level must have completed all requirements for the doctorate by the time their appointment becomes effective. Candidates at the instructor level must have completed their master's program.

The department is part of the College of Business Administration, has BBA and Master's programs as well as a doctoral program with approximately 29 Ph.D. candidates and includes 18 full-time faculty members. It is located in the heart of the Atlanta business and financial community.

Computing resources include IBM, Amdahl, and Unisys mainframes as well as DEC and IBM midrange systems, and a wide array of personal computers and graphics systems.

Salary is competitive.

Applications Deadline: January 15, 1990.

To apply—send resume to: Dr. James A. Senn, Chairman, Department of Computer Information Systems, Georgia State University, University Plaza, Atlanta, Georgia 30303. (404) 651-3880.

An Equal Educational and Employment Opportunity Institution. (03237)

### SYRACUSE UNIVERSITY
### Department Chair, Electrical and Computer Engineering

The department of Electrical and Computer Engineering at Syracuse University is seeking nominations and applications for the position of department Chair. Applications received by December 31, 1989, will receive full consideration. The appointment is to be made by July 1, 1990. The qualifications desired include: a doctorate in either electrical or computer engineering, a strong commitment to teaching and curriculum development at both the graduate and undergraduate levels, a distinguished record in research and scholarly publications, and demonstrated leadership and administrative abilities. The department consists of 45 faculty members and awards 100 BS, 200 MS, and 25 PhD degrees annually. Active areas of research include a wide spectrum of electrical and computer engineering disciplines, with an annual research budget for salaries of over $4 million. Department faculty are actively engaged in research with the New York State Center for Advanced Technology in Computer Applications and Software Engineering, the Northeast Parallel Architectures Center, the Northeast Artificial Intelligence Consortium, and the Institute for Energy Research. Applications and nominations should be submitted to Professor John Brule, Chair Search Committee, Department of Electrical and Computer Engineering, Syracuse University, Syracuse New York, 13244-1240, (315) 443-4417. Syracuse University is an Affirmative Action/Equal Opportunity Employer.

### UNIVERSITY OF CALIFORNIA AT RIVERSIDE
### Faculty Positions in Computer Science

Applications and nominations are invited for tenured or tenure track positions in Computer Science beginning July 1, 1990 or later. Ph.D. and demonstrated excellence in research and teaching are required. Prominent senior candidates are especially encouraged to apply. The program in computer science is growing rapidly, and is projected to double in size in the next 4 years. The department has decided to concentrate in areas projected to be important in the 21st century, including algorithm design, parallel computation, computational logic, design automation, programming languages, computer architecture, and software engineering. Three open rank positions are available. One is targeted to Computational Logic and another is targeted to Design Technology; the third is open as to area. This is an opportunity to participate in shaping a developing program in computer science, with the advantage of a close liaison with a well-established mathematics department.

Riverside is a rapidly growing community of over 200,000, one hour from Los Angeles; an independent metropolitan center, not a suburb. The city has its own Philharmonic and Civic Light Opera. Skiing is available from November to April less than 1 hour away in the San Bernardino mountains. Housing is far less expensive than in most other areas of Southern California. The Riverside campus of the University of California has an undergraduate enrollment of 6700 and a graduate enrollment of 1400, and is expected to double in size by the turn of the century. Other major institutions, such as UC Irvine, UCLA, USC, UC San Diego, and Cal Tech, are within easy driving distance.

Send all materials including curriculum vita and the names of at least three references to: Professor Lawrence Larmore, Chairman, Computer Science Recruiting Committee, Department of Mathematics and Computer Science, University of California, Riverside, CA 92521. The pool of candidates will consist of all those whose completed applications are received by January 8, 1990. If the search is not successfully completed from this pool, the pool will be enlarged to include all those whose completed applications are received between January 9, 1990 and March 5, 1990.

University of California, Riverside, is an Affirmative Action/Equal Opportunity Employer.

### UNIVERSITY OF SOUTHERN CALIFORNIA

Chair, Computer Science. The Computer Science Department of the School of Engineering, University of Southern California (USC), seeks a distinguished computer scientist with the vision and skill to lead a strong department and further strengthen it. The School of Engineering, with 170 faculty and 4,300 students, ranks 6th in the nation in sponsored research expenditures. The Computer Science Department has a full time faculty of 22, and a student body of 125 Ph.D. students, 250 M.S. candidates, and 200 undergraduates. The departmental research budget currently is $3M per year. Faculty research interests encompass the traditional areas of computer science, plus interdisciplinary, emerging fields such as robotics and neural computation. Computing research support is provided by a large network of modern workstations, and various supercomputers are available through the network. More than 100 SUN workstations are used for teaching. The department maintains close ties with the Electrical Engineering Department which has a strong Computer Engineering Group of 16 faculty, and with the Information Sciences Institute (ISI), an off-campus research facility of the School of Engineering. IST's staff of 200 conducts research on a broad spectrum of computer science topics. Southern California has the highest industrial production in the nation. Opportunities for industry/university collaboration are excellent because much of the local industry is high-tech and computationally oriented.

Please send nominations and applications to:

Professor Aristides Requicha
Chair, Search Committee
Computer Science Department
University of Southern California
Los Angeles, CA 90089-0782
Telephone: (213) 743-3805
Net Mail: requicha@lipari.usc.edu

Applications should include a resume and a list of professional references. USC is an equal opportunity employer.

### NEW JERSEY INSTITUTE OF TECHNOLOGY
### Computer Engineering Faculty Positions

The Department of Electrical and Computer Engineering (ECE) seeks outstanding faculty candidates at all levels for tenure-track positions in its Computer Engineering programs. These positions can begin either January or September 1990. Teaching responsibilities on undergraduate and graduate levels. The ability to conduct significant research is required, industrial experience is an asset. The department's current research interests include computer architecture, parallel processing systems, real-time operating systems, expert systems for engineering (e.g. intelligent CAD/CAE), CIM, and VLSI system design. Of 45 ECE faculty members, eight are with the computer engineering program. There are diverse modern computer facilities on campus as well as access to the von Neumann Supercomputing Center in Princeton. A microelectronics fabrication center is being constructed and a new interdisciplinary center focused on manufacturing has been formed.

Applicants must have an earned doctorate or be about to receive one in computer, electrical, or systems engineering, or in computer science wtih an undergraduate degree in engineering. Send resume with a statement of teaching and research interests and three references to: Personnel Box ECE-F.

NJIT does not discriminate on the basis of sex, race, color, handicap, religion, national or ethnic origin or age in employment.

New Jersey Institute of Technology, University Heights, Newark, NJ 07102.

### UNIVERSITY OF CALIFORNIA SAN DIEGO

The Department of Computer Science and Engineering expects to have junior level faculty positions (tenure track) in computer science and computer engineering. These positions involve research and teaching at both graduate and undergraduate levels. The department and the university offer an outstanding environment for academic computer science. For appointment at the assistant professor level, evidence of excellent potential for conducting research in computer science or computer engineering is necessary. Salary and rank will be commensurate with qualifications in conformance with University of California policies; a Ph.D. (or advancement to candidacy) in computer science or computer engineering is required. Applications received by January 31, 1990 will be considered for all positions, but later applications will also be considered if unfilled positions remain. Please send a curriculum vitae (including a statement of citizenship status) and the names of four references to:

Dr. Michael E. Saks, Chair
Faculty Recruitment Committee
Dept. of Computer Science and Engineering
Mail Code C-014
University of California, San Diego
La Jolla, California, 92093

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## BOISE STATE UNIVERSITY
## and
## HEWLETT-PACKARD

Boise State University, in cooperation with Hewlett-Packard, invites applicants for a tenure-track position in the Department of Mathematics for the fall of 1990. Applicants should have a Ph.D. in computer science or a related field, with expertise in artificial intelligence, software engineering, database systems, or operating systems. Applicants with experience in other areas of computer science will be considered. Industry experience is beneficial. Responsibilities will include teaching, research, and service at the University and at Hewlett-Packard's Boise site. Salary for 9 months is commensurate with rank and qualifications.

Boise is Idaho's largest city and is the site of many technology-based corporations. Numerous recreational opportunities exist within a short drive of the city.

A completed application, a vita, three letters of reference, and graduate transcripts are required. Contact Dr. Phillip Eastman, Computer Science Search Committee Chair, College of Arts and Sciences, Boise State University, Boise, Idaho 83725. The closing date is January 15, 1990. BSU and HP are EEO/AA employers.

## CASE INSTITUTE OF TECHNOLOGY
### NORD Professorship in Computer Engineering and Science

The Department of Computer Engineering and Science at Case Institute of Technology is seeking a nationally recognized scholar and researcher to fill the NORD Professorship. This position was recently established by the donation of one and a half million dollars, which will provide outstanding professional opportunities and a highly competitive salary, together with additional funds for travel, graduate student support and equipment. The qualifications include a Ph.D. in computer science, computer engineering or closely allied fields, and an ability to establish and develop external support for a nationally recognized research program in computer science/computer engineering. We invite applications from senior faculty at both the associate professor and full professor levels.

CWRU is a private university with a total enrollment of 8,400, of which 5,100 are graduate and professional students. The Engineering School of Case Institute of Technology is among the top ten engineering schools in terms of research funding per faculty member and undergraduate student quality. The University campus is the hub of the pleasant area known as University Circle, an incorporation with neighboring cultural centers and museums, about five miles from downtown Cleveland.

The Department of Computer Engineering and Science has 15 faculty positions, and a graduate student body of 140 students, 50 of which are in the Ph.D. program. Departmental facilities are based upon an ethernet local area network, connected to INTERNET, which supports a UNIX operating system and about 30 SUN workstations, color graphics display terminals, together with several printers. In addition, faculty and students participating in the Center for Automation and Intelligent Systems Research have access to the Center's computing facilities.

Applicants should submit their curriculum vitae and names of at least five references to: Lee J. White, Chairman, **Department of Computer Engineering and Science**, Case Western Reserve University, Cleveland, Ohio 44106; INTERNET: leew@alpha.ces.cwru.edu; applicants may wish to provide at most three reprints of their most important publications.

An equal employment and affirmative action employer.

## UNIVERSITY OF CALIFORNIA, SANTA BARBARA
### Department of Computer Science

The University of California at Santa Barbara invites applications for at least three tenure-track positions in the Department of Computer Science. These positions are available at both senior and junior levels. Senior applicants should possess extremely distinguished research records, while junior candidates should have records proving exceptional promise. The Department of Computer Science, in the rapidly expanding College of Engineering, is a strong department of 17 persons. UCSB and the College of Engineering are committed to maintaining the growth of the Computer Science Department and attaining a department having the greatest excellence and highest national visibility.

Outstanding persons in all areas of Computer Science will be considered, although the department is currently attempting to achieve its main strengths in the areas of algorithms and complexity, software systems, parallel and distributed computing, scientific computation, performance evaluation and machine intelligence. Senior appointees will have significant input in guiding the growth and development of the department. Resources will be available for state-of-the-art laboratories for research and instruction, and strong support will be made available and tailored to the needs of successful applicants. Interactions with various research groups on campus are strongly encouraged and supported.

All applicants should hold a doctoral degree in Computer Science or a related field and must have an excellent record of research. Teaching experience is highly desirable. We expect to fill these positions during the 1990-91 academic year. Positions are open until filled. Send resume and names of referees to:

Chairman, Planning and Recruitment Committee
Department of Computer Science
University of California
Santa Barbara, CA 93106

Proof of U.S. citizenship or eligibility for U.S. employment will be required prior to employment (Immigration Reform & Control Act of 1986).

The University of California is an Equal Opportunity/Affirmative Action Employer.

## MARY WASHINGTON COLLEGE
### Department of Computer Science

Mary Washington College invites applications for a tenure track position in Computer Science beginning August 1990. Preferred qualifications include a strong commitment to undergraduate teaching, a Ph.D. in Computer Science or a related field area and excellent English language communication skills. Applicants in all areas of computer science will be considered. The College and the Department of Computer Science expect its faculty to be excellent teachers, accessible to students, and to be engaged in some scholarly activity or research.

Mary Washington College is a selective, coeducational, state-supported college of the liberal arts and sciences with approximately 3300 students. The college is located in a beautiful historic area, 50 miles from both Washington, D.C. and Richmond, and near the Naval Surface Warfare Center. Opportunities abound for professional and cultural activities.

The undergraduate program in computer science is in its tenth year, enjoys an excellent reputation and graduates approximately 35 students per year. The curriculum is based upon ACM recommendations, class size in computer science is generally limited to 30 and the average class size is between 20 to 25 students. The Department has four full-time faculty and four adjunct faculty. Facilities include an Ethernet network which provides four main processors: HP 9000/850, two HP 9000/360, and Prime EXL-316, a cluster of 16 HP 9000/340 workstations and a variety of other devices. We are interested in receiving applications from qualified minorities and women. Applicants should send a resume indicating undergraduate teaching experience and areas of specialization or interest and have three references to support the applicant's professional qualifications to Ernest Ackermann, Chairperson, Department of Computer Science, Mary Washington College, Fredericksburg, Virginia 22401-5358. Consideration of applications will begin on January 5, 1990 and search will remain open until the position is filled. AA/EEO.

## ASTEM, KYOTO, JAPAN
### Research Positions in CAD and Knowledge Engineering

The newly established Advanced Software and Mechatronics Research Institute (ASTEM), Kyoto, Japan, invites applications for research and research associate positions. Speciality areas include, but are not limited to, LSI CAD, 3D CAD, and knowledge engineering. For a research associate position, a candidate should be highly qualified and hold an MS in CS, EE, or related fields; for a research position a Ph.D. is normally required. ASTEM provides an excellent environment for research in Software Engineering and AI with unique Japanese software and dedicated SUN4 and SUN3 workstations.

ASTEM is located in Kyoto, the ancient beautiful city of Japan.

Send resume to: Dr. Masanobu Matsuo, 29121 Firthridge, Rancho Palos Verdes, CA 90274; (213) 544-0855.

## UNIVERSITY OF CALIFORNIA AT DAVIS
### Faculty Positions in Computer Science

The Computer Science Division of the Department of Electrical Engineering and Computer Science of the University of California at Davis invites applicants for tenure-track positions at all ranks, in areas of distributed computing, theory, architecture, graphics, programming systems and languages.

The division is in a period of rapid growth, with the aim of becoming one of the leading computer science programs in the nation. Programs are offered leading to the Bachelor of Science, Master of Science, and Doctor of Philosophy degrees. Constantly expanding research facilities include Sequent, Encore, and Intel multiprocessor systems, several VAX systems, and numerous Sun, Microvax II, Apollo, and Iris workstations, all linked via LAN. Also available are departmental and campus instruction facilities, and the supercomputer resources of the Lawrence Livermore National Laboratories. Salary and benefits are extremely attractive.

The progressive city of Davis has a population of approximately 50,000. Located eleven miles from the state capital of Sacramento, it is an easy drive to the major cultural centers of the San Francisco Bay Area, as well as to unparalleled recreation areas, including the California coast and the Sierra Nevada mountains. The location, climate, and character of Davis make it an outstanding living environment.

Applicants should have a commitment to continued strong records of teaching and research, including the desire and ability to attract significant external support. A Ph.D. is required for all ranks. Advanced ranks require experience and accomplishments commensurate with placement. The positions are open until filled.

Respond with a resume and the names of at least three references to:

Robert M. Keller, Chair
Division of Computer Science
University of California at Davis
Davis, CA 95616

The University of California is an equal opportunity/affirmative action employer.

## UNIVERSITY OF UTAH
### Computer Science Faculty Positions

The Department of Computer Science at the University of Utah solicits applications at all professorial ranks. A candidate for Assistant Professor must earn the Ph.D. in Computer Science or related field prior to September. A candidate for Associate Professor must have, in addition, at least three years of teaching or research experience in Computer Science. A candidate for the rank of Professor must have a well-established research record in Computer Science.

The Department currently has sixteen tenure-track faculty members, two teaching faculty, as well as an additional seventeen serving in research and adjunct capacities. The student population includes approximately 200 undergraduate majors, 50 Master's degree students, and 35 Ph.D. students.

Substantially funded faculty research projects include: asynchronous computation, computer animation, computer-aided geometric design, text retrieval, computer graphics, computer system architecture, computer vision, models of computation, program verification, programming languages, robotics, symbolic and algebraic computation, theory of computation, and very large scale integrated circuit design. Funding sources include major support from DARPA, NSF, and Hewlett-Packard. Other governmental agencies and private industry also provide significant support.

The department enjoys an outstanding research environment supported by a professionally staffed research computing facility. Equipment includes: VAX 8600 and five other VAX mainframes. An 18-node BBN Butterfly parallel computer system and over 70 Hewlett-Packard, Apollo, Sun, and Silicon Graphics workstations are installed. The facility is connected to most major geographic networks (Arpanet, CSNET, USENET and Telenet). A computer graphics laboratory with equipment representative of the most advanced devices available in the industry is also available. Other specialized laboratories include facilities for image processing and understanding, robotics, parallel processing, lisp programming, computer aided instruction and VLSI research.

Applications will be considered until all positions are filled. Starting date for appointment is July 1990. Direct vita, along with the names of three or more references, by Feb. 1, 1990 or until positions are filled to:

Recruiting Committee Chairman
Department of Computer Science
University of Utah
Salt Lake City, Utah 84112

The University of Utah is an Affirmative Action/Equal Opportunity Employer and especially encourages application from women and members of minority groups.

## UNIVERSITY OF CENTRAL FLORIDA

The University of Central Florida is seeking an Associate or Full Professor of Computer Science with demonstrated expertise in object-oriented programming and computer graphics, with applications in simulation and training. Ph.D. in Computer Science or closely related discipline required. In addition to strong teaching credentials, candidates should have: (a) experience in supervising graduate student research, (b) an impressive record of attracting external support and successfully implementing research projects, and (c) substantial refereed publications in technical journals. Rank and salary commensurate with experience. Position is a joint faculty appointment between the Department of Computer Science and the Institute for Simulation and Training.

Application deadline is November 27, 1989. Qualified individuals should send a resume and list of publications to: Dr.Jerry Ventre, Institute for Simulation and Training, University of Central Florida, 12424 Research Parkway, Research Pavilion, Suite 300, Orlando, FL 32826. Equal Opportunity/Affirmative Action Employer. As an agency of the State of Florida, the University makes all search records open to the public.

## CITY COLLEGE OF CUNY
### Computer Science

City College invites applications from computer scientists committed to both teaching and research, preferably in central areas of computer science, e.g., database, operating systems, computer architecture, telecommunications, graphics, artificial intelligence, and parallel processing.

Applicants must have a Ph.D. in computer science or a closely related field. Recent Ph.D.s should have research potential and teaching experience; senior applicants should have an outstanding research and teaching record. Positions are open starting with the Spring and Fall semesters of 1990. Salary range is: $40,390 to $66,310 per academic year.

The Department offers the BS and MS degrees; the Ph.D. degree is offered in cooperation with the CUNY Graduate Center. An active research program utilizes the computing facilities of the Department, the College, and CUNY.

Screening will begin on 12/31/89, however, position will remain open until full. Please send vita and names of three references to: Daniel D. McCraken, Chair, Department of Computer Sciences, City College of CUNY, 138th Street and Convent Ave., New York, New York 10031. An AA/EEO Employer M/F/H/V.

## NORTHEASTERN UNIVERSITY, BOSTON, MA
### Dean
### College of Computer Science

Northeastern University invites nominations and applications for the position of Dean of the College of Computer Science. The Dean has administrative responsibility for all undergraduate, graduate, and research activities of the College and reports to the Provost (Senior Vice-President for Academic Affairs).

In the seven years since its founding, the College has designed and implemented an accredited undergraduate curriculum incorporating the university's cooperative education plan. At the graduate level, the College offers a Master's program and a Doctoral program, supported by a vigorous faculty research effort. The academic and research programs have the strong and continuing support of the University.

We seek to appoint a candidate who:

- is tenurable as a full professor in Computer Science
- has demonstrated excellence in research
- shows evidence of a strong commitment to education.
- has proven leadership and administrative capability
- has the credentials and capability to develop cooperative ventures with corporate and governmental partners.

Northeastern University is an affirmative action/equal opportunity/Title IX employer.

Nominations and applications should be sent to: Professor John Casey, Chair, Search Committee, c/o Faculty Senate Office, 423 Richards Hall, Northeastern University, Boston, MA 02115. CSNet Address: jcasey @corwin.ccs.northeastern.edu

## PENN STATE
### Computer Engineering

Applications are invited for tenure track faculty positions at all levels. Candidates from all areas of computer engineering will be considered, however priority will be given to those candidates in Software Engineering, VLSI, or Architecture. The Computer Engineering Program at Penn State is within the Department of Electrical Engineering which has over 50 faculty members and approximately 1300 undergraduate majors, 260 graduate students. Candidates should have a Ph.D. in Electrical/Computer Engineering or related areas. There are currently 10 faculty members within the Computer Engineering Program, and the program offers BS, MS and Ph.D. degrees in Computer Engineering. Excellent instruction and research computing facilities are available within the Department, College and at the University Computation Center. Please send letter of application, resume, or inquiries, together with three references to: Computer Engineering Program, Department of Electrical Engineering, 121 Electrical Engineering East, Box IEEE. The Pennsylvania State University, University Park, PA 16802. Deadline for applications is January 31, 1990, or until suitable qualified candidates are selected. An Affirmative Action/Equal Opportunity Employer. Women and Minorities Encouraged to Apply.

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## UNIVERSITY OF CENTRAL FLORIDA

The University of Central Florida College of Engineering invites applicants for tenure-track Assistant/Associate Professor positions in its Department of Computer Engineering. A Ph.D. in Computer Engineering or a related discipline is required, and the preferred specialty area is digital systems/computer architecture. UCF is a member of the Florida State University System and has a current enrollment of approximately 20,000 students. The University is developing a Research Park adjacent to its main campus to support high-technology government and industrial activity in the Central Florida area. Computer facilities for instruction and research include an IBM 4381, a Gould 32/6780, 2 IBM 5080 color workstations, and numerous mini and micro computers. The Department operates an Engineering AI Laboratory with 9 Symbolics Workstations and a Texas Instruments Explorer System. An Ethernet LAN using TCP/IP protocols links College of Engineering offices and labs together. Each faculty office has a private personal computer with a LAN connection.

Send curriculum vitae and the names of three references postmarked by December 1, 1989 to:

Dr. C.S. Bauer, Chair
Department of Computer Engineering
University of Central Florida
Orlando, FL 32816
Phone: (407) 275-2236

The University of Central Florida is an Equal Opportunity/Affirmative Action employer. As an agency of the State of Florida, the University makes all application materials and selection procedures available for public review.

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## UNIVERSITY OF CALIFORNIA, SANTA CRUZ

Computer Engineering at UC Santa Cruz invites faculty applications for two positions.

One Associate or Full Professor, with an application closing date of December 15, 1989. The candidate sought should have strengths in two or more of the following areas: special purpose architectures and parallel environments, computer aided design; graphics, real time systems, image processing, computer architecture, computer systems and languages, networks, and software construction (#141-889). Salary depending upon qualifications and experience.

One Assistant Professor, with an application closing date of February 1, 1990. The position is in Visualization and Scientific Computing or Computer Graphics and Workstation Architecture (#174-890). Salary range: $44,200-$48,800 (9 month basis).

A Ph.D. in Computer Engineering, Electrical Engineering, Computer Science or equivalent is required. Candidates for tenured positions must have a solid research record as evidenced by publications in technical journals. Candidates for non-tenured positions must have demonstrated research potential. All applicants will be evaluated on their research record, teaching, professional activities, demonstrated leadership in their fields, and letters of recommendation. Send applications, including curriculum vitae with cover letter, publications and teaching evaluations, 5 letters of recommendation (3 for Assistant position), promptly to the following address. Chair, Computer Engineering Faculty Search Committee, Baskin Center for Computer Engineering & Information Sciences, Applied Sciences Building, University of California, Santa Cruz, CA 95064. If any position remains unfilled after these dates, all positions will remain open at the assistant level until April 15, 1990. Please refer to Position #141-889 or #174-890 in your reply. UCSC is an EEO/AA/IRCA employer.

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## HARVEY MUDD COLLEGE
### Engineering and Computer Science

Applications are invited for a tenure track position in the Engineering Department. Appointment at the Assistant Professor level is anticipated. Applicants should have an engineering background with graduate study in computer engineering or electrical engineering and computer science and experience in both hardware and software design and development. Responsibilities will include teaching in a unified engineering curriculum, developing courses and supervising industrially sponsored projects in the Engineering Clinic. Continuing professional growth and development through research or consulting is expected; excellent opportunities exist in the local area. A doctorate in engineering or computer science is required. Industrial experience is desirable. Reply to: Professor A. Bright, Chairman, Engineering Department, Harvey Mudd College, Claremont, CA 91711. Harvey Mudd College is an equal opportunity/affirmative action employer.

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## THE UNIVERSITY OF TEXAS AT DALLAS
### Chair in Microelectronics and in Telecommunications

The Erik Jonsson School of Engineering and Computer Science is seeking applicants for a Chair in Microelectronics and a Chair in Telecommunications.

Current areas of primary focus in microelectronics are solid state devices—primarily III-V, and photonics. In telecommunications, primary focus areas are signal processing, telecommunications—primarily optical communications, computer architectures and computer networks.

Candidates must be nationally and internationally recognized leaders in their fields, and must have an exceptional record of scholarly productivity and the ability to attract research sponsorship.

The primary responsibility for the Chair holder will be to provide the leadership for a strong education and sponsored research program in cooperation with current faculty and with local high-technology industries.

Applications and nominations should be sent to:

Academic Search #708
The University of Texas at Dallas
P.O. Box 830688
Richardson, TX 75083-0688

A resume with a list of five references should be included. Applications from women and minorities are especially welcome. Indication of sex and ethnicity for affirmative action statistical purposes is requested, but not required. Non-U.S. citizens must indicate visa status. The search will remain open until both positions are filled. Inquiries should be referred to Dr. B.E. Cherrington, Dean. (214-690-2974).

The University of Texas at Dallas is an Affirmative Action/Equal Opportunity Employer.

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## SUNY STONY BROOK
### Department of Electrical Engineering

SUNY Stony Brook, invites applications for anticipated openings for all professor ranks. These positions will be tenure track with salary negotiable. The Department has undergraduate and graduate programs and extensive research activities. The areas of prime interest are computer engineering, circuit theory and applications, digital systems, pattern recognition and machine vision, computer graphics, communications and computer networking, solid-state electronics devices and circuits, VLSI design, experimental device fabrication, microwave circuits (acoustics and magnetics) and robotics. The Department has extensive computing facilities. Applicants in other areas will be considered. The Department has close relations with high technology industry. Stony Brook combines the attraction of a semi-rural location with proximity to the resources of the New York City area. Please submit resume to: Prof. Kenneth L. Short, Chairman, Department of Electrical Engineering, SUNY Stony Brook, Long Island, NY 11794-2350.

SUNY Stony Brook is an Affirmative Action/Equal Opportunity Educator and Employer. AK 220.

## HARVEY MUDD COLLEGE
### Position Announcement in Computer Science

Applications are invited for a tenure-track position in Computer Science beginning July 1, 1990. An applicant should have, or be close to completion of, a Ph.D. in Computer Science and have a strong interest in both undergraduate teaching and research. Candidates from all areas of computer science or a computer-related field will be considered. Responsibilities include teaching, research, and the supervision of industrially-sponsored projects in computer science. The Computer Science Department's facilities include a network composed of a Sequent Symmetry and two SPARCstations, a VAXstation 3100 and a VAX 11/750. The Computer Science network is also interfaced with the college network of VMS machines: a Micro VAX 2, 5 VAXstation 3100, and a VAX 8600.

Harvey Mudd College, one of the nation's most selective undergraduate colleges, is a member of The Claremont Colleges. The College is an equal opportunity/affirmative action employer. Please send resume and the names of four references to Professor Wing C. Tam, Computer Science Department, Harvey Mudd College, Claremont, CA 91711.

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## THE UNIVERSITY OF TEXAS AT DALLAS

The University of Texas at Dallas Erik Jonsson School of Engineering and Computer Science is seeking applicants for tenure track faculty positions primarily at the full professor level in its electrical engineering and engineering science programs.

Areas of primary focus are solid state devices—primarily III-V, photonics, signal processing, telecommunications—primarily optical communications, computer architectures, computer networks, computer aided manufacturing, and manufacturing science.

Applicants must have a Ph.D. in engineering or in a closely related discipline, and must have a demonstrated record of scholarly productivity and the ability to attract research sponsorship.

Responsibilities will include the establishment of a strong sponsored research program in cooperation with current faculty and with local high-technology industries, direction of master's theses and doctoral dissertations, and instruction of undergraduates.

Applications and nominations should be sent to:

Academic Search #706
The University of Texas at Dallas
P.O. Box 830688
Richardson, TX 75083-0688

A resume with a list of five references should be included. Applications from women and minorities are especially welcome. Indication of sex and ethnicity for affirmative action statistical purposes is requested, but not required. Non U.S. citizens must indicate visa status. The search will remain open until all positions are filled. Inquiries should be referred to Dr. B.E. Cherrington, Dean. (214-690-2974).

The University of Texas at Dallas is an Affirmative Action/Equal Opportunity Employer.

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## THE UNIVERSITY OF TEXAS AT DALLAS
### Head of Electrical Engineering

The Erik Jonsson School of Engineering and Computer Science is seeking applicants for the position of Head of the Electrical Engineering Program. This position is also a tenured position at the full professor level.

Candidates must be well experienced faculty members in electrical engineering programs with a strong focus on research and graduate education. In addition, the program head is expected to maintain an active research/teaching program in an area of primary importance to the program, such as solid state devices—primarily III-V, photonics, signal processing, telecommunications—primarily optical communications, computer architectures and computer networks.

Applicants must have a Ph.D. in electrical engineering or in a closely related discipline, and must have a demonstrated record of scholarly productivity and the ability to attract research sponsorship.

Responsibilities will include providing overall leadership for the academic and research functions of the program, in addition to the administrative responsibilities for the personnel, facilities, and financial aspects of the program.

Applications and nominations should be sent to:

Academic Search #707
The University of Texas at Dallas
P.O. Box 830688
Richardson, TX 75083-0688

A resume with a list of five references should be included. Applications from women and minorities are especially welcome. Indication of sex and ethnicity for affirmative action statistical purposes is requested, but not required. Non-U.S. citizens must indicate visa status. The search will remain open until the position is filled. Inquiries should be referred to Dr. B.E. Cherrington, Dean. (214-690-2974).

The University of Texas at Dallas is an Affirmative Action/Equal Opportunity Employer.

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## MEMORIAL UNIVERSITY OF NEWFOUNDLAND
### St. John's, Newfoundland, Canada
### Head
### Department of Computer Science

Applications are invited for the position of Head, Department of Computer Science, commencing on September 1, 1990. The Department has 20 full-time faculty members and offers undergraduate and graduate programmes to the M.Sc. level. Among the areas of research are software technologies, AI and expert systems, graphics, VLSI, and database systems. Some faculty hold cross-appointments to the Departments of Biology, Mathematics and Statistics, and Physics. In addition, there is a joint M.Sc. programme with the Faculty of Engineering. Departmental computing facilities currently include 3 MIPS M/120 RISC processors, several DEC MICRO-VAXes, SUN workstations and a number of personal computers, all interconnected by Ethernet and running under 4.3 BSD-UNIX. The University Computing Centre maintains a DEC VAX 8800 and three VAX-11/785/VMS-4.1 systems on a cluster, a DEC VAX 11/780 running UNIX, with access to CAD/CAM facilities. The campus is served by a fibre-optic communication network.

Applicants should have demonstrated ability in research and be able to show leadership and administrative ability appropriate to the post. The applicant should have a broad appreciation of the computer science field and be responsive to the diverse requirements of this multifaceted Department. The appointment will normally be made at the level of Full Professor, commencing on September 1, 1990.

Address applications (including the names of at least three referees) or requests for further information to:

**Dr. J.E. Strawbridge**
**Associate Dean of Science**
**(Chair, Computer Science**
**Headship Committee)**
**Memorial University of Newfoundland**
**St. John's, Newfoundland, Canada,**
**A1B 3X7**
Bitnet: JSTRAWBR@MUN.CA
Tel.: (709) 737-8155
FAX: (709) 737-4000

Applications should be received by January 15, 1990.

Memorial University encourages both men and women to apply for this position. In accordance with Canadian immigration requirements, this advertisement is directed, in the first instance, to Canadian citizens and permanent residents of Canada, but all others are encouraged to apply.

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## DREXEL UNIVERSITY
### Professor of Computer Science

The Department of Mathematics and Computer Science is seeking a distinguished computer scientist to lead the department's computer science research program. Candidates from all CS areas will be considered; areas of special interest include parallel computing, distributed systems, symbolic algebra systems, and computer graphics. The successful candidate will participate in selecting additional faculty with related interests.

The Department has 31 tenure-track faculty members in mathematics, probability and statistics, and computer science. Facilities include a network connecting the Department's Apple Macintoshes, Sun workstations and servers, AT&T 3B2 servers, and a Sequent Symmetry S-27 and a link to Drexel resources including a Convex minisupercomputer, an IBM 3090-VF, and NSFNET access.

Send a letter of application stating future research interests, a resume, and the names of at least three references to:

James C.T. Pool, Head
Mathematics and Computer Science
206 Korman Center
Drexel University
Philadelphia, PA 19104

Deadline for applications is January 31, 1990, or until the position is filled. Drexel University is an Equal Opportunity/Affirmative Action Employer.

## MASSACHUSETTS INSTITUTE OF TECHNOLOGY
### Faculty Positions

The Department of Electrical Engineering and Computer Science seeks candidates for faculty positions starting in September 1990. We anticipate openings for several junior faculty appointments for individuals who are completing, or who have recently completed, a doctorate. Faculty duties include teaching at both the graduate and undergraduate levels, research, and supervision of theses.

We are interested in candidates in most areas of electrical engineering, but opportunities in bioelectrical engineering and microwaves are extremely limited at present. In computer science, we are interested in candidates in the following two areas: Computer Systems, including operating systems, programming languages, computer architecture, databases, and graphics; and AI research in reasoning, including commonsense and qualitative physical reasoning, and reasoning using massively parallel machines.

All candidates should write to the address below, describing their professional interests and goals. Applications should include a curriculum vitae and the names and addresses of three or more references. Additional material describing the applicant's work, such as papers or technical reports, would also be helpful. All candidates should indicate citizenship and, in the case of non-US citizens, describe their visa status.

Send all applications to:

Prof. F. C. Hennie
Room 38-435
Massachusetts Institute of Technology
Cambridge, MA 02139

M.I.T. is an equal opportunity/affirmative action employer.

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## TECHNICAL DEVELOPMENT ENGINEER

Technical Development Engineer for S.W. Ohio company engaged in the development and sale of engineering software, and related consulting. Duties: Develop state-of-the-art applications and enhancements for Mechanical Computer-Aided Engineering (MCAE) and geometric modeling software products. Responsible for requirements definition, software design, code implementation, and quality assurance. Perform appropriate literature surveys to ascertain state-of-the-art approaches to the problems involved. Be prepared to prototype software to investigate implementation techniques and data structures. Utilize structured programming techniques in developing all software. Interact with other members of the technical staff to determine the development requirements to support all needed functionality. Participate in planning major software releases. Requirements: Bachelor's degree and 3 yrs. experience or Master's degree and no experience. If Bachelor's, the degree must have been in Mechanical or Electrical Engineering, Computer Science, Physics or Mathematics and experience must have included 3 yrs. in the above described duties or 3 yrs. in position(s) whose duties involved the development of mechanical engineering software for geometric modeling. If Master's, no experience is required but the degree must have been in Mechanical or Electrical Engineering, or Computer Science. (Completion of all Master's degree requirements with thesis complete except for final defense is acceptable.) For all applicants working experience or graduate level studies must have included the following, which may have been acquired concurrently (the same experience, course work or research may be used to meet more than one of these matters): (1) two years working experience involving expert systems and geometric modeling. In the alternative, acceptable are one 3 credit hr. course involving expert systems and two 3 credit hr. courses involving geometric modeling. (Geometric modeling experience or course work must have included boundary representation, constructive solids geometry and surface representations.); and (2) one year working experience or 12 credit hrs. of academic research which involved feature based modeling or feature recognition; and (3) six months working experience or 6 credit hrs. of academic research which involved C or Fortran programming. (All references to credit hours are to semester credit hours. Equivalent quarter credit hours are acceptable.) In addition, through working experience or undergraduate/graduate studies all applicants must have established MCAE research and communication skills evidenced by the following which must have concerned MCAE: two research reports or two academic publications (one report and one publication are acceptable), or a completed graduate thesis (except for final defense is acceptable). Hours & pay: 40 basic hrs., 8 a.m. to 5 p.m., plus varied overtime hours (5-10 average) per wk.; $35,600 to $45,000 salary per yr., depending on education and experience, plus annual discretionary bonus usually averaging approximately 5% of salary. Qualified applicants reply immediately with resume (NO CALLS) to R. Lechler, JO #1099649, Ohio Bureau of Employment Services, P.O. Box 1618, Columbus, Ohio. 43216.

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## HARVEY MUDD COLLEGE
### Engineering and Computer Science

Applications are invited for a tenure track position in the Engineering Department. Appointment at the Assistant Professor level is anticipated. Applicants should have an engineering background with graduate study in computer engineering or electrical engineering and computer science and experience in both hardware and software design and development. Responsibilities will include teaching in a unified engineering curriculum, developing courses and supervising industrially sponsored projects in the Engineering Clinic. Continuing professional growth and development through research or consulting is expected; excellent opportunities exist in the local area. A doctorate in engineering or computer science is required. Industrial experience is desirable. Reply to: Professor A. Bright, Chairman, Engineering Department, Harvey Mudd College, Claremont, CA 91711. Harvey Mudd College is an equal opportunity/affirmative action employer.

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## THE UNIVERSITY OF TENNESSEE SPACE INSTITUTE
### Graduate Research Assistantships and Post-Doctoral Research Appointments

Applications are invited for graduate research assistants and post-doc research appointments in computer science, particularly in artificial intelligence, expert systems and neural networks. UTSI offers M.S. and Ph.D. degrees in computer science with emphasis on artificial intelligence.

The half-time research assistantships are granted on a nine-month basis with a stipend ranging from $9,000 to $11,500 plus waiver of a $1,710 maintenance fee and a $2,952 out-of-state tuition fee. Summer appointments may also be available. Post-doc salary is open. To receive an application or for further information please contact: Edwin Gleason, EdD, Assistant Dean for Admissions & Student Affairs, The University of Tennessee Space Institute, Tullahoma, TN 37388 (Phone: (615) 455-0631, ext 247).

UTSI is an AA/EEO employer.

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## THE UNIVERSITY OF ARIZONA
### Department of Computer Science

Invites applications for faculty positions at all ranks to begin in August, 1990. Applicants must have a doctorate in Computer Science or a closely related field. Applicants for senior positions should have made substantial research contributions to the field, while applicants for junior positions should show promise of future excellence.

There are currently 14 faculty members, with plans to expand over the next few years. Research is currently conducted in a variety of areas including Algorithm Design and Analysis, Complexity Theory, Databases, Distributed and Parallel Computing, Graphic and User interfaces. Operating Systems, Programming Languages, and Scientific Visualization. Qualified individuals working in these areas—as well as other areas, such as artificial intelligence, computer architecture, performance analysis—are encouraged to apply.

The research program is supported by numerous grants to individual faculty as well as a second department-wide NSF infrastructure grant. Computational facilities are diverse, including a Sequent Symmetry, dozens of Sun workstations, VAX 8650, an Intel iPSC Hypercube, an HP 9000 graphics workstation, a NeXT machine, and dozens of Macintoshes. Also available are high-resolution color terminals, a QMS color PostScript printer, laser printers, and a phototypesetter.

Send a complete resume and the names of at least three references to:

**Udi Manber**
**Faculty Recruiting Committee Chairman**
**Department of Computer Science**
**The University of Arizona**
**Tucson, AZ 85721**

Applications will be reviewed beginning January 15, 1990, but the positions will remain open until filled.

An equal opportunity/affirmative action employer.

### UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN
### The Department of Computer Science

The Department of Computer Science, University of Illinois at Urbana-Champaign, anticipates possible tenure, tenure-track appointments in several disciplines. Applicants must have outstanding academic credentials and an ability to teach effectively at both the graduate and undergraduate levels. Selected candidates will be expected to initiate and carry out independent research and to perform academic duties associated with our BS, MS, and PhD programs. Since the department is large, several vacancies are filled each year. A continuing search is conducted throughout the year to fill open positions. All applications received by December 1, 1989, will receive equal consideration, although a search will continue until a position has been filled. All candidates judged as qualified for a position will be interviewed. PhD or imminent completion required. Salary open, based on qualifications. Starting dates are January 6, 1990 or August 21, 1990, although other dates are negotiable. Send resume including names of three references to: C.W. Gear, Head, Department of Computer Science, 1304 W. Springfield Avenue, Urbana, IL 61801. Phone (217) 333-6454. The University of Illinois is an affirmative action, equal opportunity employer.

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### UNIVERSITY OF OTTAWA
### OCRI/NSERC Research Chair
### Multimedia Databases
### Department of Electrical Engineering

The Ottawa Carleton Research Institute (OCRI) and the Natural Sciences and Engineering Research Council of Canada (NSERC), in collaboration with the Telecommunications Research Institute of Ontario (TRIO), BNR, Bell Canada, Digital Equipment of Canada Ltd. Gandalf Technologies Inc. and Leigh Instruments Ltd., are sponsoring the

OCRI/NSERC Industrial Research Chair
In
Real-Time Multimedia Distributed
Database Systems

The position is a tenure-track one. The successful candidate will be appointed at the full Professor level in the department of Electrical Engineering at the University of Ottawa, a major bilingual University in Canada and a principal partner in the Telecommunications Research Institute of Ontario (TRIO), a Center of Excellence. The Department of Electrical Engineering has currently 24 full-time professors, 9 adjunct professors, 107 graduate and 381 undergraduate students. The Chairholder will interact with the Multimedia Communications Research Group of the department, currently composed of 33 researchers, funded at an annual rate of $1 million and carrying leading-edge research in the area. The Chair award includes funding for one reseach associate, one research assistant, two graduate students, two co-op technicians and equipment. An extensive Multimedia Communications laboratory is available. The Chairholder and the research team will interact with the industrial sponsors of the Chair. Cross-appointment with the Department of Computer Science is envisaged.

REQUIREMENTS: Candidates should have a Ph.D. in Electrical or Computer Engineering, or Computer Science and at least five years experience in or with an industrial environment. Experience in research and development in relational database management systems, multimedia communications, distributed architectures, multimedia documents and interfaces is required. The candidate should present evidence of high scientific productivity and quality, through refereed publications and/or other indicators more appropriate to his/her industrial background.

Employment equity is a University policy. In accordance with Canadian immigration laws, priority will be given to Canadian Citizens or permanent residents.

Applications, including a detailed curriculum vitae and names of three references should be sent to:

The Chairman
Department of Electrical Engineering
University of Ottawa
Ottawa, Ontario, Canada, K1N-6N5
Tel. (613) 564-2495

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### UNIVERSITY OF CALIFORNIA, DAVIS
### Faculty Positions in Electrical Engineering and Computer Science

The Department of Electrical Engineering and Computer Science at UC Davis invites applications for tenure track positions at all ranks. The primary areas of interest are image processing and computer vision; optoelectronics; and computer engineering and microprocessor applications.

The department, with 50 faculty members and 180 full-time graduate students, is experiencing rapid growth. Our College is the nation's sixteenth largest producer of engineering Ph.D.'s in a University which has the nineteenth largest extramural research funding. Salary and benefits are extremely attractive.

Davis is a pleasant, family-oriented community near Sacramento, within easy driving distance to Silicon Valley, the Lawrence Livermore National Laboratory, San Francisco, the Pacific Ocean, and the Sierra Nevada Mountains.

We are seeking individuals with strong records of teaching and research and with ambitious plans. Senior appointments require outstanding records of achievement; junior apppointments must show evidence of great promise. All faculty are expected to have a strong commitment to teaching at all degree levels, and to demonstrate the ability to attract significant research support.

The positions require a Ph.D. degree or equivalent, and are open until filled. Send a resume and the names of at least three references to:

Professor S. Louis Hakimi, Chair
Attention: Faculty Search Committee
Department of Electrical Engineering
and Computer Science
University of California
Davis, CA 95616

The University of California, Davis, is an equal opportunity/affirmative action employer.

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### CLARKSON UNIVERSITY

The Department of Mathematics and Computer Science at Clarkson University invites applications for tenure track positions in computer science. Ph.D. in computer science or a closely related discipline is required. Rank and salary are negotiable. We are looking for candidates who will enjoy teaching both graduate and undergraduate courses, and who will add research strength to the computer science program. Strong candidates in all areas are encouraged to apply. We are especially interested in new colleagues with interests in complexity theory and theoretical aspects of programming languages and systems.

Clarkson University is a small selective technological university with a strong research tradition. The department offers BS and MS degrees, as well as the option of a Ph.D. in mathematics with emphasis in computer science. Computing facilities in the department include a cluster of Sun workstations in faculty offices and labs, connected via campus-wide ethernet to numerous other machines as well as to regional and national networks such as NYSERNet and Internet.

The university is located in upstate New York close to the scenic Adirondack and Thousand Island regions. The concentration of college campuses in the vicinity creates a rich cultural environment with a high quality of life without the problems of major cities.

Applications including vita and names of three references should be submitted to Professor A. Fokas, Department of Mathematics and Computer Science, Clarkson University, Potsdam, NY 13676. Clarkson University is an equal opportunity/affirmative action employer and encourages applications from women and minorities.

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### UNIVERSITY OF WASHINGTON

The Department of Computer Science and Engineering expects to have one or more tenure-track openings starting in the 1990-91 academic year. We seek outstanding applicants who add to our existing research strengths, particularly in graphics, programming languages/compilers, and software engineering, or who bring significant new research strength to our department.

A moderate teaching load allows time for quality research and close involvement with students. We expect applicants to have a strong commitment to both research and teaching, and an outstanding record of research for their level.

The department may also have several visiting positions that would require both teaching and research. It may be possible to hold these for portions of the 1990-91 academic year.

Interested applicants should send a letter of application, a resume, and the names of four references to Paul Young, Faculty Recruiting Committee, Department of Computer Science and Engineering FR-35, University of Washington, Seattle, Washington 98195.

The University of Washington is an Affirmative Action/Equal Opportunity Employer. The Ph.D. is required for these positions.

### OREGON GRADUATE CENTER

Would you like to work in an academic environment with an active graduate education program, but with no undergraduate teaching responsibilities? A place that encourages serious research by providing strong administrative support and excellent facilities? If so, consider joining the growing faculty of the Oregon Graduate Center's Department of Computer Science and Engineering.

We seek both senior and junior faculty colleagues with experience in graduate education and ambitious research goals. Technical areas of particular interest include: computer architecture, VLSI design, artificial neural networks, distributed database systems, and parallel computation.

OGC is located in Portland, one of the most affordable of the West Coast's beautiful cities. Portland's relaxed life style and intense work style combine to offer you a setting in which both your family and your research can thrive.

For more information about OGC, please address inquiries to: Professor Richard Kieburtz, Chairman, Department of Computer Science and Engineering, Oregon Graduate Center, 19600 NW von Neumann Drive, Beaverton, OR 97006.

OGC is an equal opportunity employer.

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### WAKE FOREST UNIVERSITY
**Department of Mathematics and Computer Science**
**Department of Radiology**
**Assistant/Associate Professor of Computer Science and Radiology**

Applications are invited for a tenure-track joint position in the Department of Mathematics and Computer Science and the Department of Radiology. Candidates at the level of Assistant Professor or Associate Professor will be considered. A Ph.D. in computer science or equivalent is required.

Primary research responsibilities should focus on applications of image analysis and image processing in Radiology. The ideal candidate should have experience and interest in medical image processing/analysis, parallel computations and high speed computing for imaging applications. Additional expertise in the areas of computer graphics, artificial intelligence, computer architecture and communications is desirable. A demonstrated ability to attract research funding is essential.

Teaching responsibilities will include one undergraduate computer science course per semester. An undergraduate major in Computer Science is currently offered and a master's degree in Computer Science is currently being developed in the Department of Mathematics and Computer Science. A master's and doctorate degree in Electrical and Computer Engineering with emphasis on medical applications is being offered through a research program sponsored jointly by the Bowman Gray School of Medicine and North Carolina State University with the degree awarded by N.C. State University.

The image processing laboratory in the Department of Radiology supports a number of Sun 4 workstations, an AT&T 3B20, a stand-alone MRI workstation, an AT&T Pixel Machine and several terminals and PC's. The workstations and the 3B20 are part of the state-wide extended Ethernet operated by the Microelectronics Center of North Carolina with access to Internet, Bitnet and other wide area networks. The lab is housed in the new MRI building which has two Picker 2T MRI scanners and a third GE unit is scheduled to be installed in the first quarter of 1990. Research time is available on the MRI units as well as on a fully integrated clinical PACS.

Available in the Department of Mathematics and Computer Science are SUN 4 workstations and various microcomputers networked via Ethernet, the university's Prime 4150 and AT&T 3B15, and access to CSNet and LINCNET. Several parallel computing machines based on transputers will soon be available. Currently a plan is being implemented to connect the Reynolda Campus of Wake Forest to the Bowman Gray Campus via the extended Ethernet operated by MCNC.

Applications and inquiries should be sent to: Dr. Douglas Maynard, Chairman of Computer Science/Radiology Search Committee, Department of Radiology, Bowman Gray School of Medicine, Wake Forest University, Winston-Salem, North Carolina 27103.

EOAA employer.

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### ALMA COLLEGE
**Director of Computer Services**

Search is extended for Director of the Herrick Computer Center at Alma College, open immediately. Responsibilities include planning, directing, managing, and implementing modern and dynamic services for a selective liberal arts college of 1200. Facilities include a VAX cluster with varied attached workstations, stand-alone and networked MacIntosh and MS-DOS micro-computers, and an Ethernet which connects the VAX cluster with over 40 microcomputers (network nodes) and other facilities (via terminal servers). Diverse instructional applications include computer science major, cognitive science program, all departments and offices, and extensive word processing. Apple HEPP II program and automated (DYNIX) library system are operational; QUODATA administrative software system is being installed. Five-member staff operates the equipment, developes applications, provides training and manages installation and maintenance services.

A Master's Degree, working knowledge of VMS, demonstrated managerial skills and experience with a varied user community required. Send full credentials and three letters of recommendation to Ronald Kapp, Provost, Alma College, Alma, Mi. 48801. Review of candidates will begin after November 1. An equal opportunity, affirmative action employer, actively seeks applications from women and minorities.

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### THE UNIVERSITY OF TEXAS AT ARLINGTON

The Department of Computer Science Engineering at The University of Texas at Arlington invites applications for tenure-track or visiting faculty positions in all areas of computer science or computer engineering. Applicants with expertise relating to reliable real-time distributed systems, telecommunications software, object-oriented systems, machine vision, knowledge-based systems, or parallel processing will be given highest priority. Rank is open. An earned doctorate or equivalent and a commitment to teaching and scholarly research are required. Openings are expected for September 1990. Applications received prior to March 1, 1990 will receive full consideration. Interested persons should send a resume to Bill D. Carroll, Professor and Chairperson, Computer Science Engineering Department, P.O. Box 19015, The University of Texas at Arlington, Arlington, TX 76019. Phone 817-273-3785. FAX 817-273-2548.

The University of Texas at Arlington is an Equal Opportunity Affirmative Action Employer.

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### UNIVERSITY OF MISSOURI-ROLLA
**Computer Science Faculty Positions**

The Computer Science Department at the University of Missouri-Rolla invites applications for tenure-track positions at all levels. Applicants for senior positions should have demonstrated significant research and teaching abilities. A doctorate in Computer Science or a closely related area is required.

The Department grants B.S., M.S., and Ph.D. degrees and has well-equipped Departmental computing laboratories which complement extensive university facilities for research and instruction.

The University of Missouri-Rolla emphasizes science and engineering, has about 5,000 students, and is situated in a non-urban environment in the Ozarks. Applicants will be accepted until the positions are filled. Please send a resume containing the names of three references to: Search Committee, Computer Science Department, University of Missouri-Rolla, MO 65401.

UMR is an Equal Opportunity/Affirmative Action Employer.

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### COMPUTER DESIGN ENGINEER

Computer Design Engineer in research & development division for employer in central Ohio to design & construct databases for a system that gathers, stores & analyzes traffic data from telephone switches using a distributed processor architecture. No experience required. Must have Ph.D. in computer science with graduate work concentrating in distributed data bases & object-oriented computer algorithms for multiprocessors. 40 hours per week, (work schedule: 7:45am - 4:30pm). Salary is $52,000 per year. Qualified applicants send resume (NO CALLS) to G. Maugans, JO# 1213291, Ohio Bureau of Employment Services, PO Box 1618, Columbus, OH 43216.

### UNIVERSITY OF MARYLAND

Computer Vision/Human-Computer Interaction: Assistant, Associate and Full Research Scientists to direct advanced research programs in computer vision or human-computer interaction. One year renewable positions whose availability and continuation are dependent on contract/grant funds. Depending on the area of research, Ph.D. in computer science, psychology, or closely related discipline required. For computer vision positions, experience in computer vision research required, specifically in areas such as three-dimensional and time-varying scene analysis, robot navigation, knowledge based vision systems, and computer architectures for vision. For human-computer interaction positions, experience is required in areas such as development of user interfaces and human factors testing. Salary up to $60,000 depending on level of position. Closing date for accepting applications is September 1, 1990. Indicate which position and for which area of research you are applying and submit signed and dated curriculum vitae plus three references to: Barbara Hope, Center for Automation Research, University of Maryland, College Park, MD 20742-3411. AA/EOE.

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### UNIVERSITY OF LOUISVILLE
### Engineering Mathematics and Computer Science Positions

The School is seeking qualified individuals for engineering computer science position, assistant/associate professor, tenure track starting the 1990-91 academic year. Requirements include Ph.D. with specialization in Computer Science, Computer Engineering, or in Engineering. Candidates should have teaching and research interests in Computer Vision, Database Design, Computer Networking, Robotics Languages, Parallel Computing, Software Engineering, or Artificial Intelligence. Candidates having interests in closely related areas will be considered.

Strong preference will be given to candidates with an engineering background. Responsibilities include research and the teaching of graduate and undergraduate courses. Excellent computing facilities are available including DEC 8650 VAX with a VAX Cluster; 2-IBM 3081; and Vision Systems, a VAX based sound system, graphics equipment, AI Symbolics and DEC workstations, and micro systems in departmental laboratories in a local area network. The Department offers Masters of Engineering in Computer Science and Ph.D. degree in Computer Science and Engineering. Expected start date is August 15, 1990. Applications will be accepted until position is filled.

Send application letter indicating Visa Status and resume to:

Dr. Khaled A. Kamel, Chairman
Department of Engineering Mathematics
and Computer Science
Speed Scientific School of Engineering
University of Louisville
Louisville, Kentucky 40292
EO/AA

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### IUPUI, INDIANAPOLIS, IN
### Chairman, Computer and Information Science

The Department of Computer and Information Science at Indiana University—Purdue University at Indianapolis (IUPUI) is currently seeking applications for the position of Department Chair.

IUPUI (established in 1969) is a large urban university (its current enrollment is 26,800 students) with programs in Art, Business, Dentistry, Education, Engineering and Technology, Health, Journalism, Law, Liberal Arts, Medicine, Nursing, Physical Education, Public and Environmental Affairs, Science, and Social Work. The department consists of 10 full-time faculty members. It offers Bachelor and Master degrees, and is expected to develop a Ph.D. program in the near future. The research interests of the faculty include artificial intelligence, artificial neural networks, computer graphics, computer vision, databases, fault-tolerant computing, information theory, motion analysis, numerical analysis, pattern recognition, and speech recognition.

The university supports computing with a network of IBM and VAX mainframes, and with several clusters of microcomputers. Department computing is done on a ring of the university computing network; department facilities include a microvax file server, numerous faculty workstations, a research laboratory, and an instructional laboratory.

Indianapolis, the capital of Indiana, is a pleasant city in which to live. It is a city in which there are numerous opportunities for joint work with federal, state, and local government, and local industry. It is a city in which the cost of living is relatively low, and in which there are many cultural and sports attractions.

The review of applications is in progress, and will continue until the position is filled. Please send nominations and applications to:

Office of the Dean of Science
School of Science
IUPUI
1125 East 38th Street
Indianapolis, IN 46205-2810

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### UNIVERSITY OF MARYLAND UNIVERSITY COLLEGE
### Faculty for Europe and Asia

Planning a sabbatical or leave of absence? The University of Maryland University College seeks excellent lecturers for undergraduate computer science, computer applications, and information systems management courses on U.S. military bases in Europe and in Asia and the Pacific. Renewable annual appointments begin August 1990. Minimum requirements include a master's degree in computer science or a related field, recent college teaching experience, and U.S. citizenship. Benefits include transportation and military base privileges. Frequent travel and the cost of schooling make these positions difficult for those with children. Send resume to Dr. Ralph E. Millis, Overseas Programs, The University of Maryland University College, College Park, MD 20742-1642. AA/EEO.

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### SAN JOSE STATE UNIVERSITY
### Department of Mathematics and Computer Science

A tenure track faculty position in computer science is available for candidates holding a Ph.D. by August, 1990. The Ph.D. in computer science is preferred, but a Ph.D. in any of the mathematical sciences, together with substantial teaching/research experience in computer science, may also be acceptable. Rank and salary commensurate with experience.

The Department offers baccalaureate and masters degree programs in computer science, applied and pure mathematics, statistics, and mathematics education.

Applications completed by January 2, 1990 will receive full consideration. Send vita, three letters of reference and transcripts to Dr. Veril Phillips, Chairman, Department of Mathematics and Computer Science, San Jose State University, San Jose, CA 95192-103. EEO/AA SCI 90-05.

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### UNIVERSITY OF SOUTHERN CALIFORNIA

The Computer Engineering Division of the Department of Electrical Engineering-Systems at the University of Southern California is expanding and looking to fill positions at the Assistant, Associate, and Full Professor level in the following areas: VLSI, Robotics, Performance Modelling, Knowledge Engineering and Design Automation. The highest priority areas are VLSI and Robotics and we would welcome applications at the Associate or Full Professor level in these areas. For all openings, please send a resume and the names of at least three academic references to Jerry M. Mendel, Chairman Department of Electrical Engineering-Systems, University of Southern California, Los Angeles, CA 90089-0781. USC is an equal opportunity/affirmative action employer.

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### JACKSON STATE UNIVERSITY
### Department of Computer Science

The Department of Computer Science at Jackson State University in Jackson, Mississippi invites applicants for three (3) Tenure Track positions at the rank of Assistant Professor. A Ph.D. in Computer Science or related discipline is preferred; Master of Science in Computer Science (ABD) considered. The starting date is January 1990. Salary is competitive and negotiable and is commensurate with background and experience. The Assistant Professor will teach 12 hours per semester at the undergraduate and graduate level, conduct research, advise students and serve on appropriate committees. Please send letter of interest, resume, and three references to:

William L. Lupton, Chair
Department of Computer Science
Jackson State University
1400 JR Lynch St.
Jackson, MS 39217
(601) 968-2105

Jackson State University is an Equal Opportunity Affirmative Action Employer.

### WRIGHT STATE UNIVERSITY
### DAYTON, OH
### Assistant to the Chair
### Department of Computer Science and Engineering

An instructor is sought to assist the chair in administration of the department, instructional programs, student affairs and contracts. Applicants must have at least an MS in computer science, computer engineering or a relevant discipline plus experience or desire to mainly perform administrative duties in a university environment.

The department offers BS, MS and Ph.D. degrees in computer science and computer engineering. It has 25 Ph.D. faculty, 10 instructors, 30 GTAs and GRAs, 700 undergraduate students, 50 Ph.D. students and a rapidly growing research contract base, currently at $600,000 per year. Wright State is located adjacent to Wright Patterson Air Force Base.

Please submit a detailed resume including names of 3 references to Dr. Alastair D. McAulay, NCR Distinguished Professor and Chair, Department of Computer Science and Engineering, Dayton, OH 45435. CSNET: amcaulay@wright.edu.

Reviewing will begin on November 22, 1989, and continue until the position is filled or January 1, 1990.

WSU is an equal opportunity/affirmative action employer.

### LOUISIANA STATE UNIVERSITY
### SHREVEPORT

Position available, graduate and undergraduate teaching responsibilities. Background in computer hardware preferred, but progressive department can make use of any Ph.D. level specialty. Be part of Louisiana's renaissance. Call 1-318-797-5302 or write Dr. William Mitchell, Chair, Computer Science Department, LSU-Shreveport, One University Place, Shreveport, LA 71115. LSU-Shreveport is an affirmative action/ equal opportunity employer.

### CLEVELAND STATE UNIVERSITY

The Department of Computer and Information Science at Cleveland State University has a tenure track position in the areas of distributed systems or software engineering and design. Responsibilities include teaching (two courses/quarter) & research. Salary is very competitive. Qualifications: Ph.D. in Computer Science, MIS, or a closely related field. Ph.D. candidates with substantial progress on a dissertation will be considered. Close relationships to business, engineering, and other departments provide an environment conducive to research and consulting. In addition to university computing facilities, the department has laboratories using VAX computers running UNIX, VMS, and state of the art software. Faculty offices are equipped with personal computers. Inquiries and vita should be sent to: Dr. James D. Schoeffler, Chairperson, Computer & Information Science Dept., Cleveland State University, E. 24th & Euclid Ave., Cleveland, OH 44115. Equal Opportunity Employer, m/f/h.

### UNIVERSITY OF CALIFORNIA, LOS ANGELES
### COMPUTER SCIENCE DEPARTMENT

The Department of Computer Science at the University of California, Los Angeles, invites applications for tenure-track positions at the Assistant Professor level in Computer Science beginning in July 1990. Applicants should possess the Ph.D. in Computer Science by July 1990. Applications are also welcome from highly distinguished candidates at the senior level.

Quality is our key criterion for selecting applicants. We expect them to have a strong commitment to both research and teaching and an outstanding record of research for their level. It is important that they exhibit strong potential for continued excellence in university research.

We seek applicants in any mainstream area of Computer Science and we particularly welcome those with research strength in software related areas.

Interested applicants should send a letter of application, a resume, and the names of four references to:

Professor Wesley W. Chu, Chair
Computer Science Department
Attn: Ms. June Myers
Boelter Hall 3732
University of California, Los Angeles
Los Angeles, CA 90024-1596

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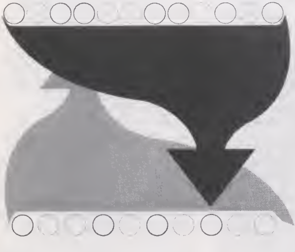

# IJCNN-90-WASH-DC

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# BOOK REVIEWS

Editor: Guy Johnson, School of Computer Science, Rochester Institute of Technology, Rochester, NY 14623.

## *Tips & Techniques for Using Low-Cost & Public Domain Software*

John Gliedman (McGraw-Hill, New York, 1989, 387 pp., $24.95)

This useful book isn't deeply technical, but it could overwhelm most novice PC users. It seems better aimed at the user who is no longer awed or intimidated by the machine, who is growing impatient or frustrated waiting for the machine, or who wants things done differently or more easily. This user is at least vaguely aware that there is software that could make his or her PC more useful, but doesn't have the time (or perhaps the inclination) to keep abreast of the market.

This author does a good job of winnowing the thousands of offerings to an acceptable — though still not very short — menu of choices. In addition, he provides lots of information, and often instruction, about the recommended items. The book will certainly guide the reader to more-satisfying and less-expensive choices than are likely without it. One caveat: The PC software world is fiercely competitive and rapidly changing, so much of the material will be obsolete in a year or two.

This is supposed to be a highly opinionated book, and the author has the background to offer opinions authoritatively. I found his frequent metaphors and analogies a bit annoying, but they might make the book more readable for a less-technical audience. (Such "light touches" seem rather common in PC books; maybe editors like them.)

Unfortunately, the book reflects a hazard of desktop publishing: its usefulness is impaired by many errors. The author explains that he typeset the book himself using Ventura Publisher, and it seems as though nobody else proofed the book. The spelling is impeccable; the words are just used incorrectly. Many of the errors will offend only perfectionists; the intended meaning is clear, the misinformation will do the reader no harm, or the error is an obvious typo. Other errors are serious enough to damage the user's confidence in the book.

In particular, the potentially excellent chapter titled "A Selective Guide to MS-DOS 2.XX and 3.XX" is made useless by errors in the sample DOS commands and the explanation of DOS behavior. Some of these reflect the author's naivete in certain areas; others are just catastrophic typos. The author clearly has a broad background in microcomputers dating back to the CP/M era, but his knowledge in a number of areas is either incomplete or erroneous.

**The PC software world is fiercely competitive and rapidly changing, so much of the material will be obsolete in a year or two.**

Much of the rest of the book is devoted to how-to-do-it information for the various software packages, but the integrity of the information is damaged by the early errors. This may not be of great consequence, since the author's information is really necessary in only a few cases. It is mostly just a sampler of the documentation and on-line help that accompany the programs.

On the plus side, the author has done a great deal of valuable work in reviewing at least several hundred of the thousands of PC software packages available and identifying many of the best of them. I agree with most of his recommendations. Prices and suppliers' names and addresses are provided in all cases. General information also includes libraries, bulletin boards, and other central sources.

The book emphasizes software but also devotes a chapter to selected hardware enhancements. Most of these are designed to make your PC faster, and their inclusion reflects the author's description of himself as a "PC hot-rodder." The recommendations are well chosen, but he offers only limited guidance toward cost-effective solutions for individual users.

The book emphasizes software utilities and tools to enhance the PC operating environment. This is a much narrower spectrum than the title suggests. Two major application areas, databases and spreadsheets, are not addressed at all. The book does cover two of the best shareware word processors and generously covers telecommunications. Also, the chapter titled "Software Speedups" offers many inexpensive ideas for making life with a PC less frustrating.

Deservedly, the author devotes a whole chapter plus an appendix to Extended Batch Language. This powerful RAM-resident program enhances DOS's rather primitive batch processor to allow control of almost any combination of application programs and activities, including stacking of automatic responses to questions asked by programs. Although the EBL program comes with comprehensive documentation, the tutorial in the book and the examples in the appendix go far toward selling the reader on the program.

The chapter on menu programs and other aids for managing PC operations highlights some of the best offerings. It also illustrates why books devoted to PC software have such short-lived usefulness. For example: The author highly recommends PKARC as the best available set of file compression utilities — the shareware standard. However, as the book was being printed, PKARC became obsolete as the result of a lawsuit. Upgrades will no longer be offered. But a new, superior utility family by the same author is rapidly being implemented by bulletin board sysops and other shareware sources across the country.

The chapter on the Microsoft Mouse programming language — devoted entirely to building mouse menus — seems to exist only because the author has a Microsoft Mouse. It doesn't try to sell the virtues of life with a mouse, and it offers a rather disinterested discussion of the language's capabilities and limitations. The

PC mouse population includes several vendors with their own mouse drivers and languages. The user's choice is typically based on such factors as cost, functionality, and feel. Also, many application programs and newer operating system shells include mouse drivers. This chapter would have been more valuable if it had offered a review of the diverse mouse offerings, their capabilities, compatibility, and comparative technology. Such treatment is even more susceptible to early obsolescence than is the software material, but the essence of it still would have been valuable.

The chapter on multitaskers and task-switchers provides excellent coverage and effectively conveys that such tools are well avoided unless they offer real payoffs for specific situations. Multitasking under DOS is a risky business best reserved for well-tested sets of well-behaved application programs with clear performance benefits (e.g., down- or uploading files in the background while editing text or doing something equally innocuous in the foreground). The book properly notes that DOS's print.com is one of the most useful, best performing, and cheapest (free) mini-multitaskers around.

For the CP/M diehard, the author includes 10 pages on low-cost hardware and software to make your favorite CP/M programs and disks usable on your PC.

Communications programs and machine-machine transfers get massive treatment, ranging from the simple but serviceable comm.bas (free with DOS/Basic demos) to importing alien files using the CopyIIPC Deluxe Option Board. Additional material covers Trojan horses and disk and file repair.

Matching the enormous array of printer hardware to the even greater array of PC software, and making the printer do everything it's supposed to do, is the most formidable task in setting up new software. Printer vendors universally regard this as the software vendor's problem and rarely provide instructions comprehensible by the average user. The author's efforts only nibble at the problem. Instead, he spends considerable effort detailing the tedium involved in generating graphic images. His approach differs from that of most printer manuals, but it is not any easier to understand. The exposition does make clear why the reader may be interested in several appropriate utilities.

Although I am disappointed in the high error count, I commend the author for his massive effort and recommend the book for those PC users who are somewhere between novice and guru. Even pros may enjoy matching wits with the author, or maybe seeing how many errors they can find. But buy the book soon — it will become a bit more obsolete every month.

Charles B. Stott
Tucson, Ariz.

## *Expert Systems in Engineering Design*

Michael D. Rychener, ed (Academic Press, Boston, 1988, $34.95)

This book defines an expert system as "a computer program that is largely a collection of heuristic rules (rules of thumb) and detailed domain facts that have proven useful in solving the special problems of some technical field." As such, an expert system can be

(1) a knowledge base in which strategies, models, rules, and concepts are stored;
(2) an inference engine that instigates and controls searches and makes inferences (i.e., improves the knowledge base by learning); and
(3) a user interface.

This book reports a number of case studies from Carnegie Mellon University's Engineering Design Research Center. The studies are grouped under the headings "Synthesis : The Generation of Alternative Designs," "Expertise: The Nature of Expert Decisions," and "Integrated Software Organization."

The editor offers these case studies as the basis for further research leading to a science of design. Specific design areas covered include architecture, catalyst selection, electronic design, metallurgy, environmental studies, and software engineering.

The studies were intended to identify and mechanize those rules that make an expert an expert. Does such work endanger the existence of human experts? Probably not. In fact, by mechanizing routine decision making, designers should be able to concentrate on serious problems without getting buried in everyday detail.

Do designers welcome such an environment? Not necessarily; some do, some don't. But it is coming anyway, and this book prepares the way.

James C. Hammerton
Rochester Institute of Technology

## *Ideas and Information: Managing in a High-Tech World*

Arno Penzias (W.W. Norton & Co., New York, 1989, 219 pp., $17.95)

Penzias' book is interesting, but not a must.

The author provides a good explanation of information and telecommunication technology. He covers one topic per chapter, and though each chapter can be read independently of the others, the book really should be read sequentially. The book's style and organization make it interesting and valuable for both professionals and casual readers. Technical knowledge is not needed to read the book.

Penzias leads the reader through basic information-processing concepts; numbers, words, and pictures; rules and programming languages; information machines versus conventional machines; modern technology; intelligence; ideas; the implications of information; and the human element in the information world.

The author focuses on the potential benefits of various uses for information and telecommunication. He achieves his stated objective of "making [the book's] readers more comfortable with technology and better able to profit from it."

If you have the time, and if you agree that information and telecommunication technology will shape our future, then you should read this book.

Israel Borovits
Tel Aviv University

## *Algorithm Animation*

Marc H. Brown (MIT Press, Cambridge, Mass., 1988, 186 pp., $30)

"Every reader will remember something different from this thesis," the author states in this ACM Distinguished Dissertation for 1987. More specifically, although this book will be of particular value to graphics designers and college instructors, it contains material of interest for those people working in object-oriented programming, operating systems, and even compiler design.

As a college professor, I jealously long for a teaching workstation like the prototype "electronic classroom" that Brown describes: a system to graphically illustrate, compare, and contrast the dynamic flow of algorithms. The capabilities of this system far surpass earlier efforts that provided videotape capabilities. The systems developed at Brown University (Balsa-I) and by Brown for his graphics dissertation (Balsa-II) include not only large-screen projection in the classroom, but also individual Macintosh workstations for each student. The system has been used extensively at Brown University in courses on data structures and advanced algorithms, among others.

The pedagogical dream incorporated in the design was for the typical class period to be half lecture, half student experimentation in a lab setting. The system has not been used in this fashion for a variety of educational reasons, but the evolutionary development of this system by Brown and others makes interesting reading and provides insights into future design options.

Brown's book describes the state of this research and classroom animation system. He focuses on the project's background, design considerations, related research, and evolutionary development, plus compromise limitations of the current version and future research directions. He also describes the significant planning and scripting effort by the animators and "algorithmaticians" who are the system's client-programmers.

Brown begins with an introduction to the scope of his work, specifically pointing out that algorithm animation is not the same as, but certainly related to, recent developments in visual programming. Chapter 2 plus two appendixes clearly identify background and related projects. The Balsa-I and Balsa-II systems are described from several perspectives, including those of the system developers and author/users in Chapters 3-5. Chapter 4 contains a particularly good definition of scripts: "a record of an end-user's session that can be stored . . . and replayed." Brown describes the design of scripts and their use and potential. As in so much of his thesis, he takes time to point out other application possibilities for the script concept. This is part of what will make this thesis worthwhile for many readers.

Chapter 6 details the implementation of Balsa-II and its differences from Balsa-I, concluding with a conscientious evaluation of the work's strengths, limitations, and future research requirements. Brown closes in Chapter 7 with a concise but helpful projection of the use of his work and future research directions for expansion and exploration.

The writing is usually clear and crisp, although an occasional sentence must be reread to clearly understand its intent. A few typos have slipped through, but none of them is seriously distracting or confusing. One minor irritant is the author's decision to capitalize Pascal and all computer languages except Smalltalk. Finally, the index is helpful, if incomplete.

Appropriately, Brown makes unusually effective use of visuals and graphics — not only of the expected data structures and graphics displays, but also of the system design and code. Unfortunately, the displays are all monochrome, thus requiring the reader to invest his or her imagination to appreciate the aesthetics of and information provided by the color displays.

An interesting aspect of this work is the use of the Macintosh Toolkit as one of its major building blocks, along with previous research done in Smalltalk. Nevertheless, the Balsa projects will be of value to researchers and developers using a variety of software tools and hardware including workstations and parallel processors. Some inferences can even be made about future graphics hardware needed to support improved performance in such algorithm animation systems.

This system is tremendously powerful, albeit expensive and resource intensive. It would have been interesting for the author to project when such systems will be economically viable for the computer science classroom and typical research laboratory, but such a prediction would probably be outdated and inaccurate already.

In summary, this short thesis should be of interest to those dealing with any aspect of graphics design and algorithm development. By inference, the book has much to say about the future requirements and needs for standardized graphic user interfaces. Prospective readers are encouraged to at least peruse it for the ideas and topics it stimulates.

R. Waldo Roth
Taylor University

# NEW LITERATURE

**Heterogeneous databases.** The integration of existing information systems entails a careful analysis of many technical, organizational, and strategic issues. *Integration of Information Systems: Bridging Heterogeneous Databases*, edited by Amar Gupta, lists key issues and specifications. The book, a volume in the IEEE Press Selected Reprint Series, is published under sponsorship of the IEEE Computer Society.

The 334-page volume is$59.95 for IEEE members, $79.95 for nonmembers. For more information, contact the IEEE Service Center, 445 Hoes Lane, Piscataway, N.J., 08855-1331. Specify order No. PC0242-8.

**Neural computing simplified.** In *Neural Computing: Theory and Practice*, author Philip D. Wasserman offers an introduction to artificial neural networks for the nonprofessional. The 240-page book assumes no mathematical background beyond an undergraduate scientific education. The basics are covered in the first two chapters and specific networks are covered in their own chapters.

The book is $36.95. Contact Von Nostrand Reinhold, Mail Order Dept., PO Box 668, Florence, KY 41022-0668, phone (606) 525-6600.

**Computer vision.** In *Computer Vision for Electronics Manufacturing* (ISBN 0-306-43182-3, 250 pp., $50 in the US and Canada, $60 elsewhere), L.F. Pau analyzes specific applications for vision in electronics manufacturing and relates them to image-processing sequences. The book is aimed at manufacturing engineers and at vision reserachers.

Contact Plenum Publishing, 233 Spring St., New York, NY 10013-1578.

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① 이력서 우측상단에 지원분야 및 지원부문을 기재하고 개별통지 가능한 전화번호, 주소를 명기 바람.
② 자기소개서는 가족사항, 성장배경, 담당업무 및 직책, 주요업적 등을 포함하여 구체적으로 작성바람.

**SAMSUNG**
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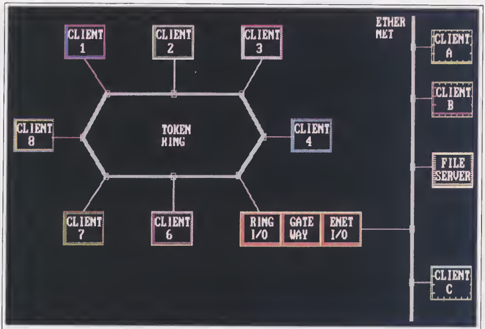
**NEW FOR LAN PLANNERS**



Realistic simulation of your Local Area Network, quick results --no programming

# SIMLAN II now predicts performance of LAN's

## Free trial and, if you act now, free training

SIMLAN II uses simulation to predict your LAN performance. You simply describe your LAN and workload.

**Animated simulation follows immediately--no programming delays.**

**Easy-to-understand results**

You get an animated picture of your LAN. System bottlenecks and changing levels of utilization are apparent.

You can model clients, servers, bridges and gateways.

Your reports show system statistics such as transfer times, information throughput, and message loss. Client, server, and gateway statistics show queue lengths, waiting times, and blocking.

**Computers with SIMLAN II**

SIMLAN II is available for most PC's and Workstations.

**Your network simulated**

You can predict the performance of any LAN. Industry standard protocols such as Ethernet, Token Ring, Token Bus, and FDDI are built-in. Others can be modeled.

You can easily study the effect of changing parameters or even protocols.

Seeing your LAN animated increases everyone's understanding of its operation and builds confidence in your results.

**Free trial information**

The free trial contains everything you need to try SIMLAN II™on your computer. For a limited time we also include free training **--no cost, no obligation.**

Call Paul Gorman at (619) 457-9681, Fax (619) 457-1184. In Europe, call Richard Eve on (01) 528-7980, Fax (01) 528-7988.

## Free trial offer

See for yourself how SIMLAN II quickly answers LAN performance questions.

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**Return to:**
CACI Products Company
3344 North Torrey Pines Court
La Jolla, California 92037 IEEE COMP
**Call Paul Gorman at (619) 457-9681.**
**Fax (619) 457-1184.**

**In Europe:**
CACI Products Division
Regent House, 89 Kingsway
London WC2B 6RH, United Kingdom
**Call Richard Eve on (01) 528-7980.**
**Fax (01) 528-7988.**

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